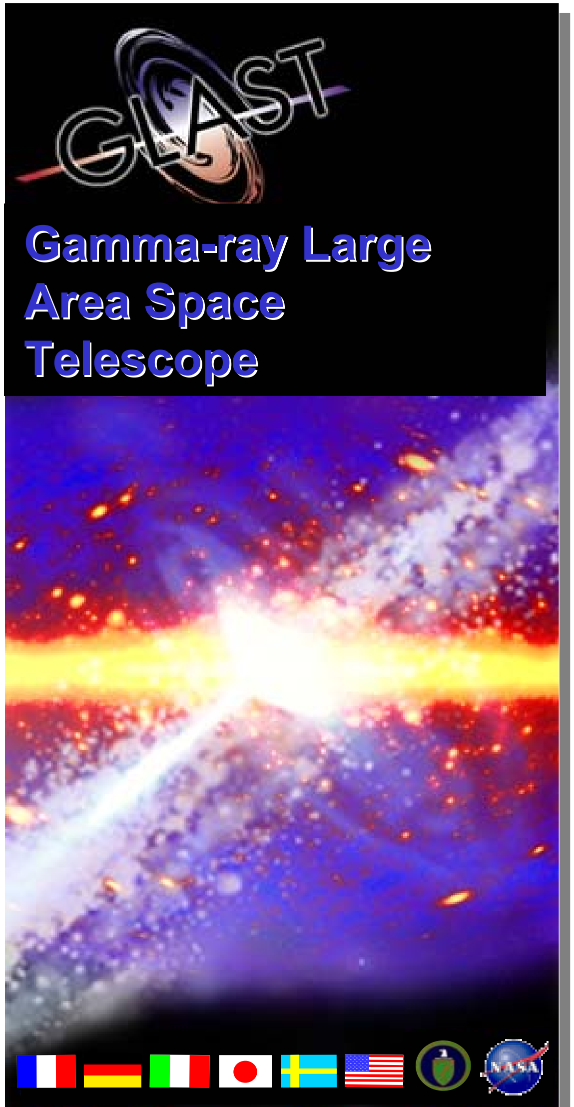


GLAST Large Area Telescope:

AntiCoincidence Detector (ACD)

CDR

January 2003

Michael Amato

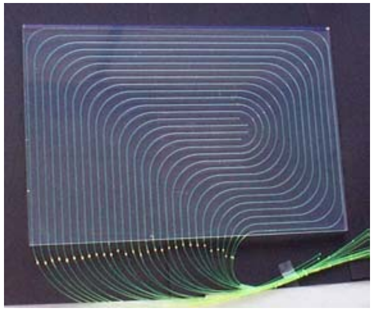
ACD Systems Engineering

Outline

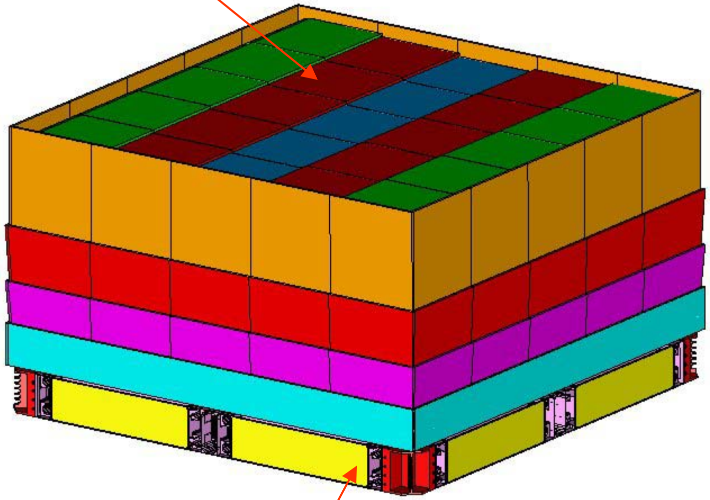
- System Overview
- Requirements and Systems Documentation
- Interfaces
- Design Decisions/Major Trades
- Verification
- Risk
- Technical Issues and Status

System Overview

Prototype ACD tile read out with Wavelength Shifting Fiber



Tile Shell Assembly (TSA)

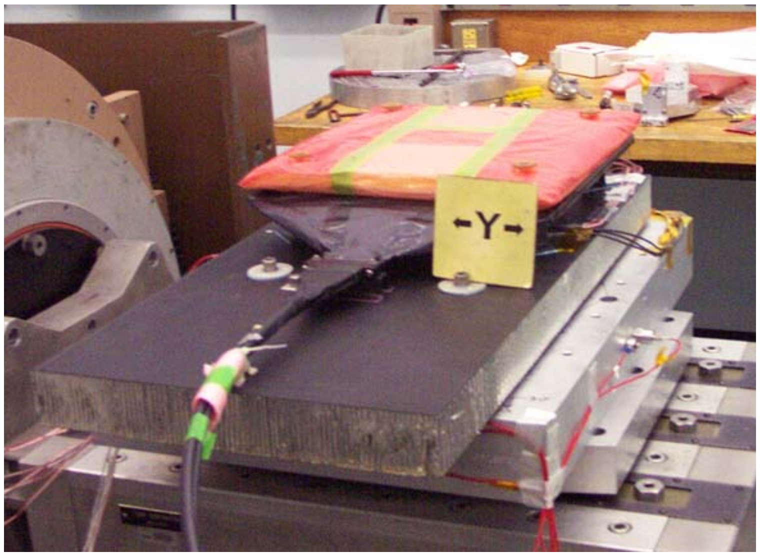


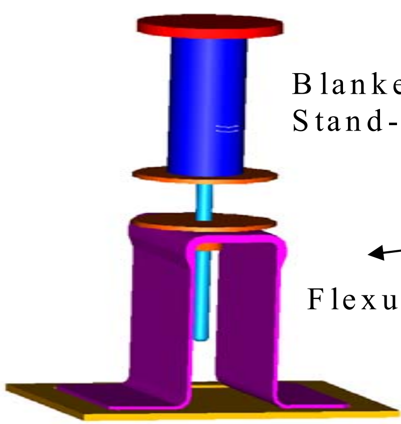
Base Electronics Assembly (BEA)

- TILE SHELL ASSEMBLY
  - 89 Plastic scintillator tiles
  - Waveshifting fiber light collection (with clear fiber light guides for long runs)
  - Two sets of fibers for each tile
  - Tiles overlap in one dimension
  - 8 scintillating fiber ribbons cover gaps in other dimension (not shown)
  - Supported on self-standing composite shell
  - Covered by thermal blanket + micrometeoroid shield (not shown)
- BASE ELECTRONICS ASSEMBLY
  - 194 photomultiplier tube sensors (2/tile)
  - 12 electronics boards (two sets of 6), each handling up to 18 phototubes. Two HVBS per electronic chassis

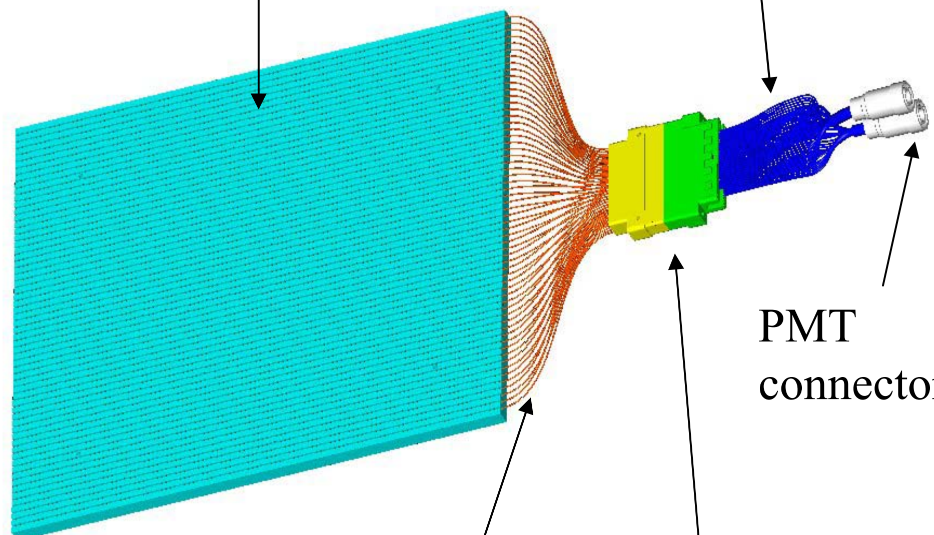
System Overview

- **<u>Tile Detector Assembly (TDA)</u>**





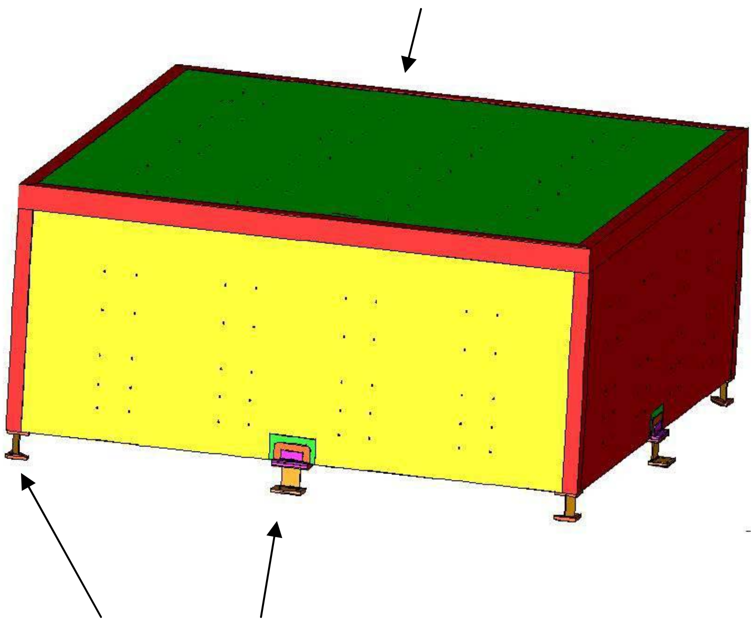
Flexures (4 per tile)



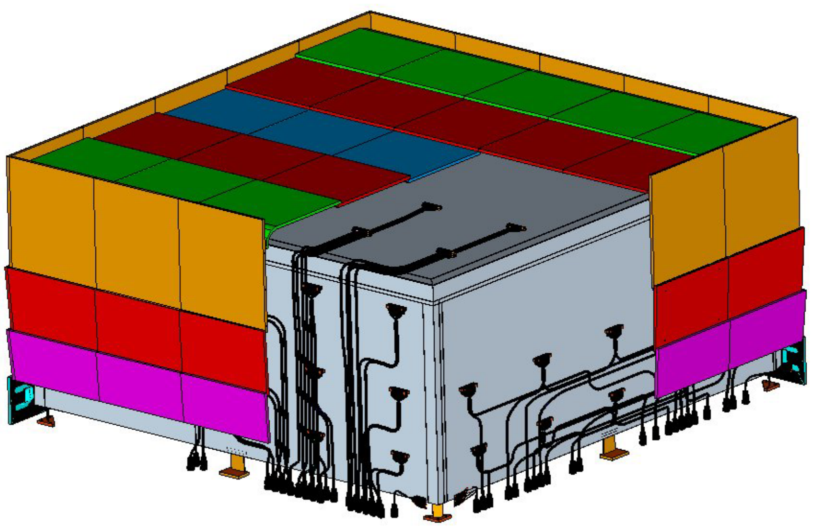
System Overview

- **<u>Shell & Tile Shell Assembly (TSA)</u>**

Composite Shell



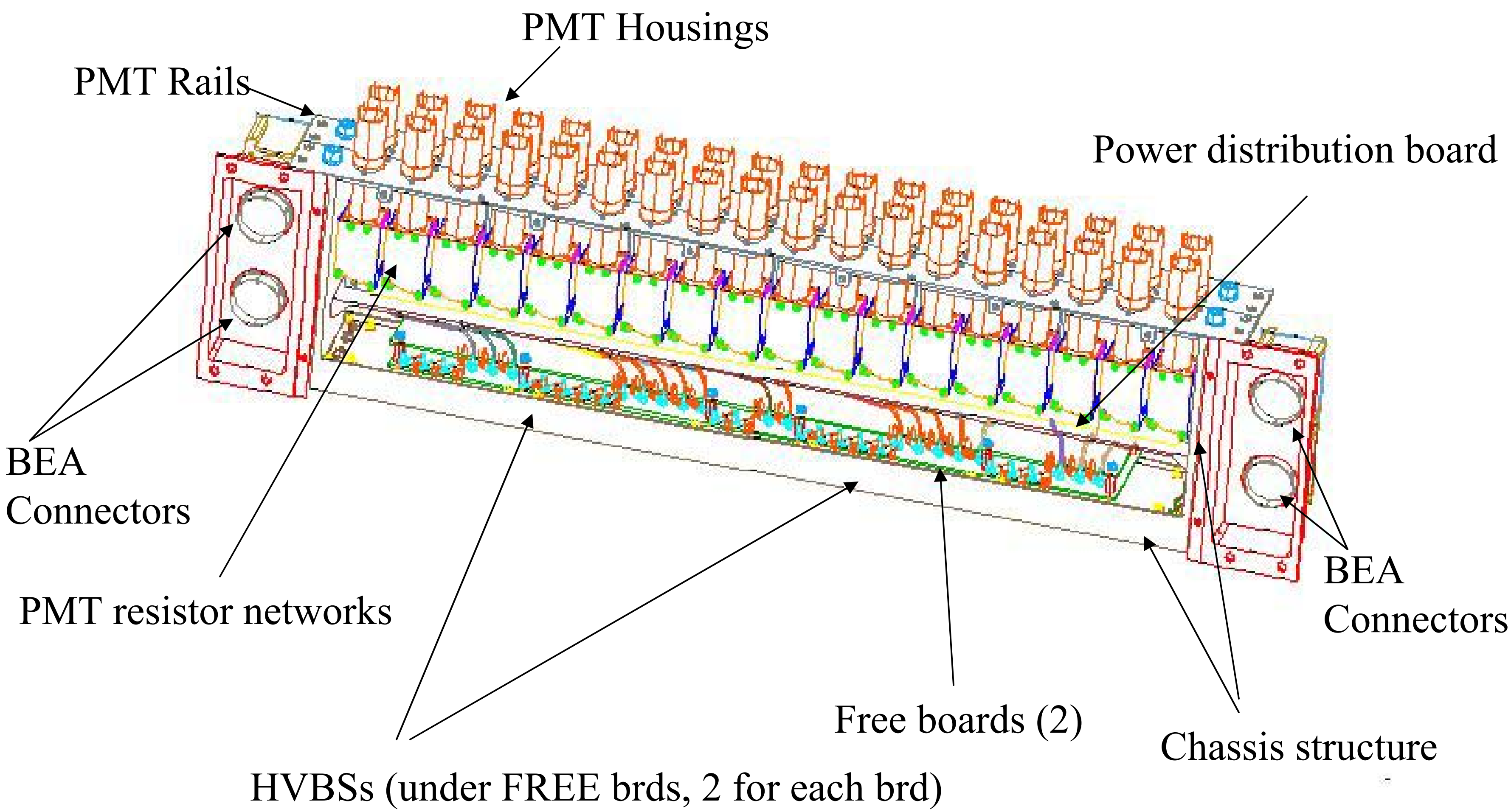
Flexures to Base Frame



TDAs on Shell become the TSA

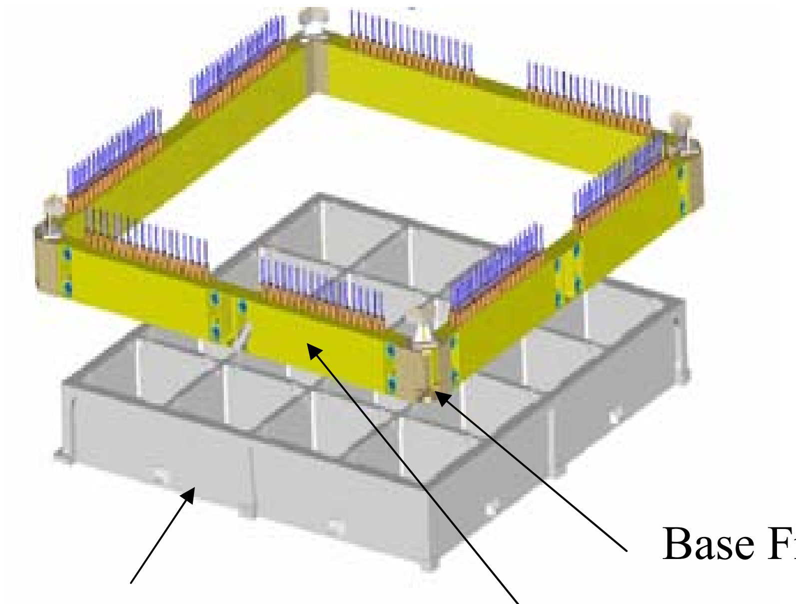
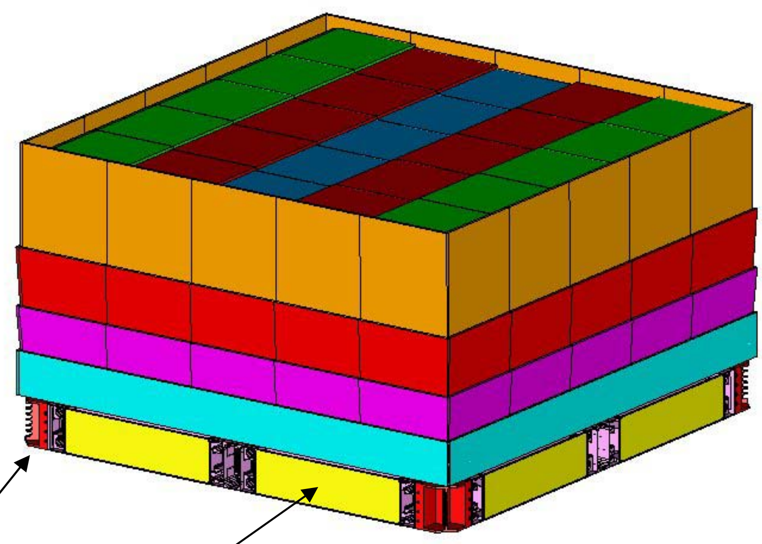
System Overview

- **Electronics Chassis**

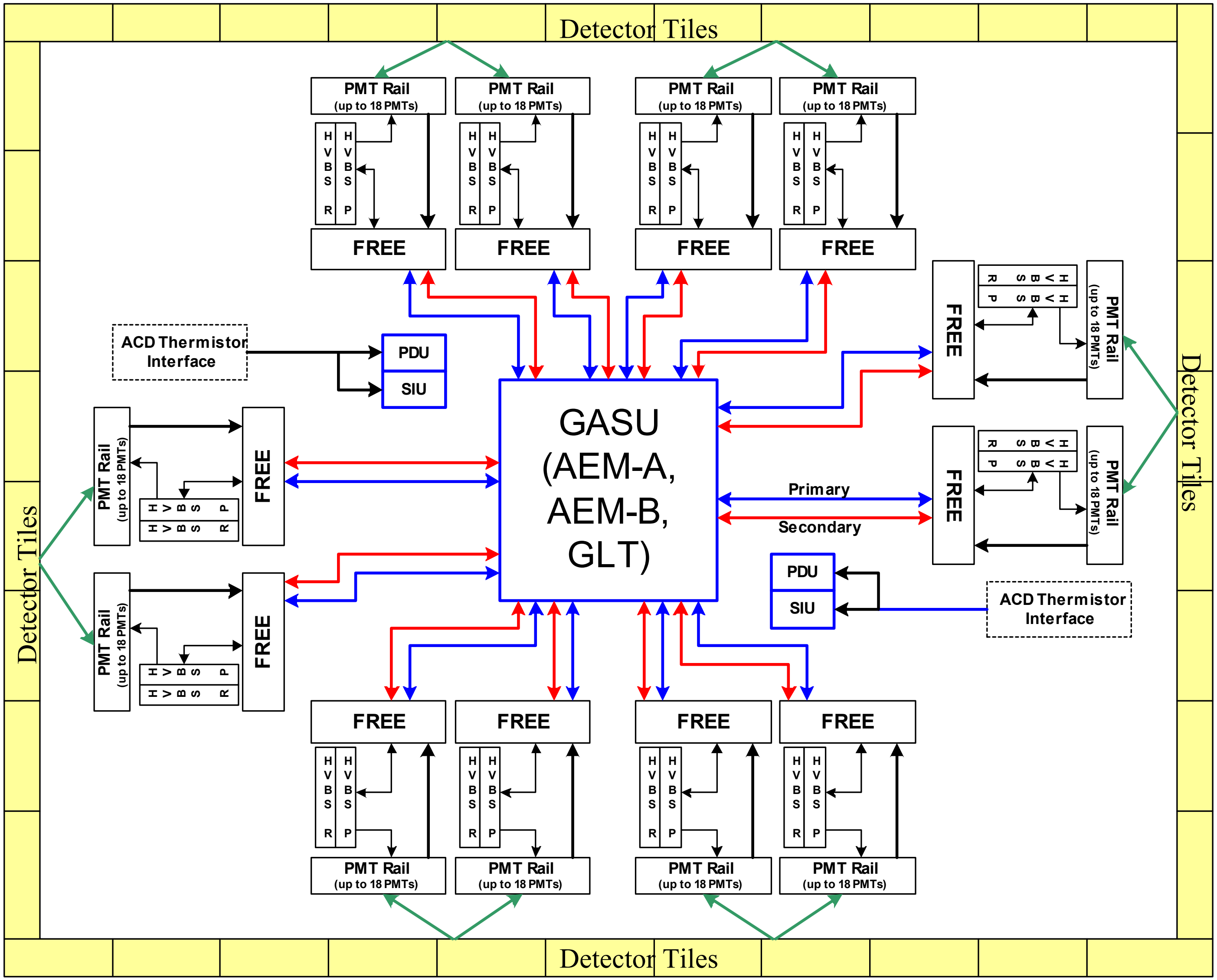


System Overview

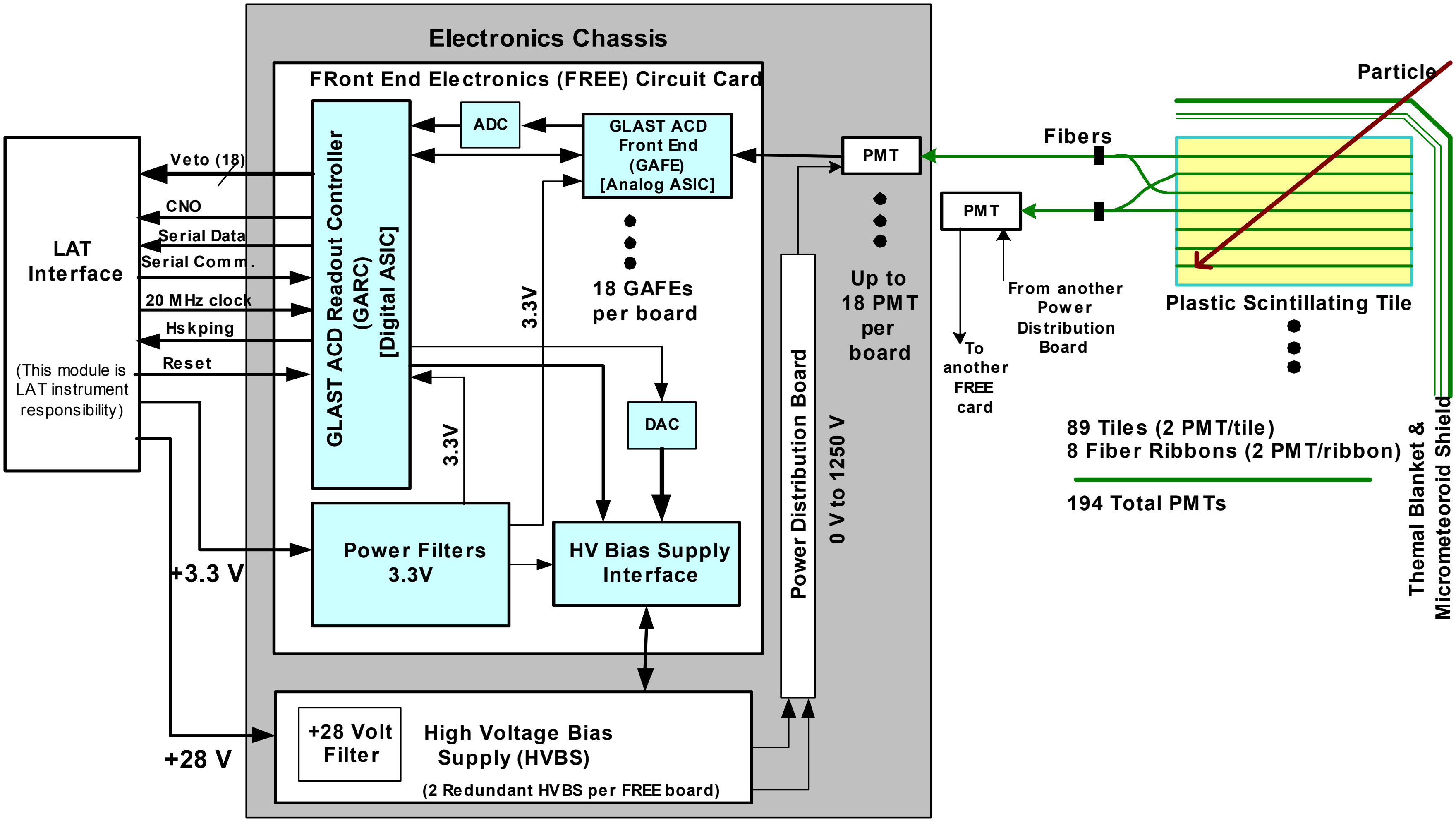
- **Base Frame Assembly becomes Base Electronics Assembly with electronics chassis installed**

System Overview



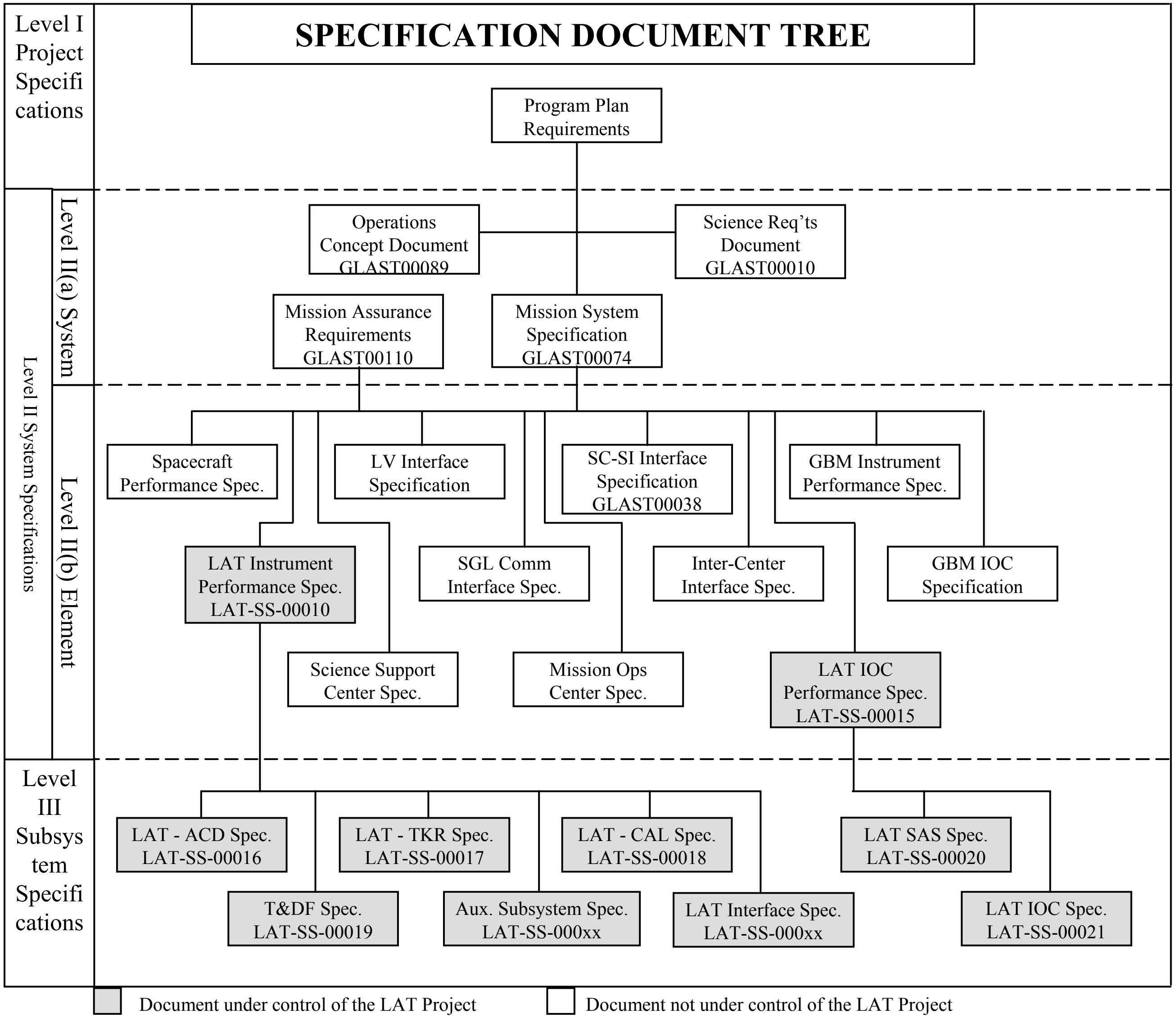
System Overview



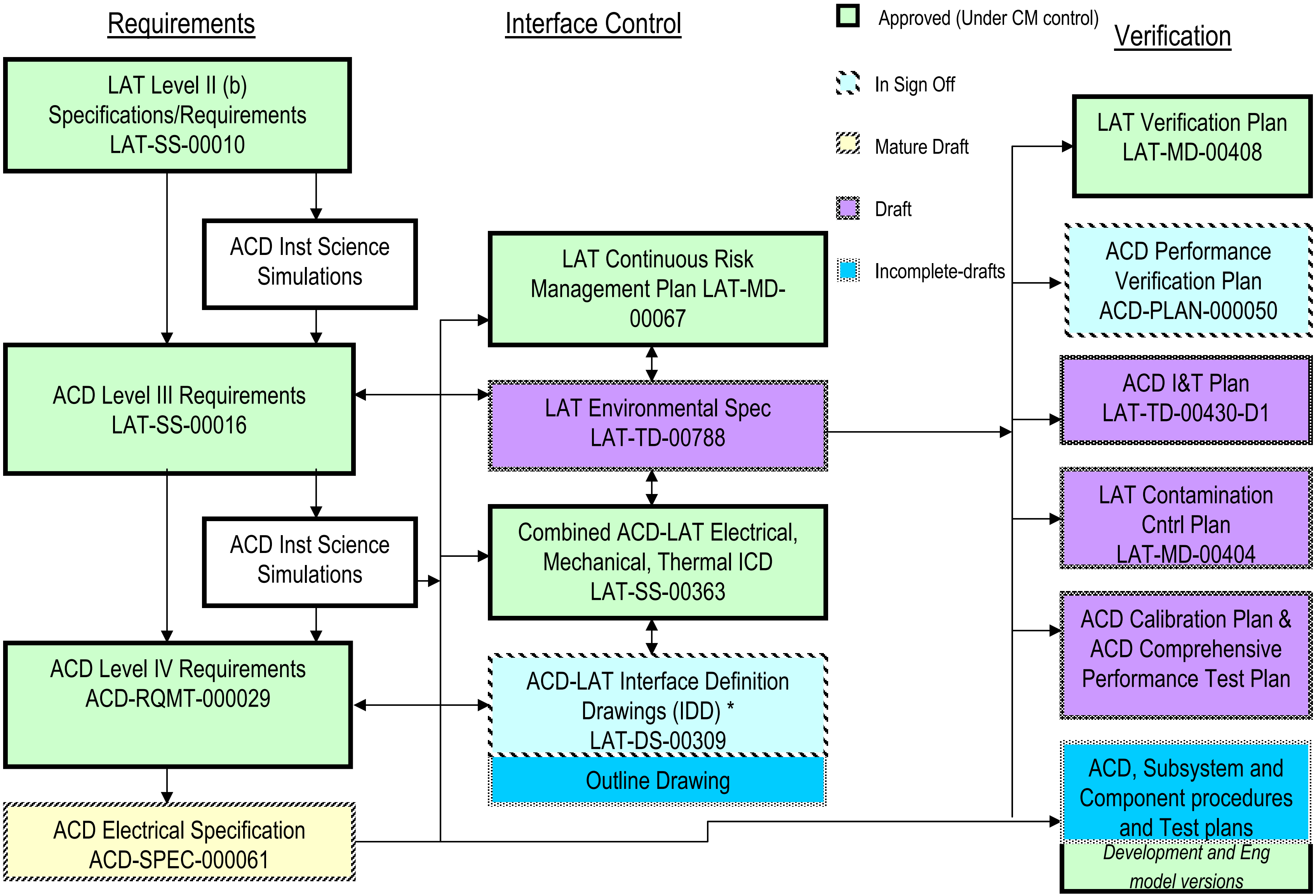
REQUIREMENTS

(& SYSTEMS DOCUMENTATION)

GLAST Requirements Flow



ACD Requirements Flow/Relationships



ACD Requirements Database

- ACD uses our Requirements Database in DOORS to Track Requirements

ID	LAT ACD Subsystem Level III Requirements, LAT-SS-00016	Parent req Link Comments	Link Action Items
	other sources from which they derive are listed in the Requirements Table below.		
ACD3-15	**5.2 Detection of Charged Particles**		
ACD3-16	The ACD shall detect energy deposits with energies of above an adjustable threshold nominally at 0.3 MIP (minimum ionizing particle) (see 5.3 below) and produce VETO signals.		
ACD3-17	**5.3 Adjustable Threshold on Detecting Charged Particle**		
ACD3-18	The threshold for VETO detection of charged particles shall be adjustable from 0.1 to 2.0 MIP, with a step size of ≤0.05 MIP. (0.1 to 0.6 MIP would have been range if no degradation was expected)		
ACD3-19	**5.4 Detection Efficiency**		
ACD3-20	The average detection efficiency for minimum ionizing particles shall be at least 0.9997 over the entire area of the ACD (except for the bottom tiles on each side, for which the efficiency shall be at least .99 , simulation confirmation of this number is desired at some point).		Latest GAP analysis h been sent to Alex for e simulation update
ACD3-21	**5.5 Instrument Coverage**		
ACD3-22	The ACD shall cover the top and sides of the LAT tracker down to the top of the CsI. The top of all 4 sides of the ACD scintillator shall be extended upward so as to be at least as high as the highest point in		

ACD Level III Requirement Database (DOORS)

Active Links between Requirements

ACD-LAT ICD DOORS Database

Active Links between Requirements

ID	LAT ACD Subsystem Level IV Requirements and Verification Table, LAT-SS-00352	In-links at depth 1	Req Action item	Req
ACD4-89	**5.10.5 HVBS Input Power**			
ACD4-90	Each HVBS shall operate from a supply voltage of 28V ± 1V, with possible input ripple of 10 mV (frequency range 50 Hz to 50 MHz). The noise shall be less than 100 mV RMS from DC to 1.0 MHz.	ACD ICD LAT-SS-00363 ACDICD-45		
ACD4-91	**5.10.6 HVBS Line and Load Regulation**			
ACD4-92	The HVBS output voltage shall be regulated to ±0.5% for all combinations of input voltage and load current. (This produces ~5% change in PMT gain).	ACD Level III Requirements LAT-SS-00016 ACD3-18 ACD Level III Requirements LAT-SS-00016 ACD3-20		
ACD4-93	**5.10.7 HVBS Output Ripple**			
ACD4-94	The HVBS output voltage ripple shall be compatible with the ACD ASIC design. The HVBS output voltage ripple shall not exceed ±2 mV p-p over the frequency range 100 Hz to 50 MHz	ACD Level III Requirements LAT-SS-00016 ACD3-16		

ACD Level IV Requirement Database (DOORS)

Level III Key Requirements Summary

Reference: LAT-SS-00016

Parameter	Requirement	Expected Performance	Verification Method
Detection of Charged Particles	**≥ 0.9997 average detection efficiency over entire area of ACD (less for bottom row of tiles)**	**≥0.9997** **≥0.99 (bottom tiles)**	**Test and Analysis**
Fast VETO signal	Logic signal 200-1600 nsec after passage of charged particle	200-1600 nsec	Demonstrate
PHA signal	For each phototube, pulse height measurement for each Trigger Acknowledge (TACK) Below 10 MIP, precision of <0.02 MIP or 5% (whichever larger) Above 10 MIP, precision of < 1 MIP or 2% (whichever larger)	< 0.02 MIP or 5% < 1 MIP or 2%	Test and Analysis
False VETO rate - backsplash	**< 20% false VETO's due to calorimeter backsplash at 300 GeV**	**< 20%**	**Test and Analysis**
False VETO rate - noise	< 1% gamma-ray rejection from false VETO's due to electrical noise	< 1%	Analysis
High Threshold (Heavy Nuclei) Detection	Detection of highly-ionized particles (C-N-O or heavier) for calorimeter calibration.	Yes	Analysis
Size	Outside: 1796 x1796 x 1050 mm 1806 x 1806 for lowest 310mm Inside Grid: 1574 x 1574 x 204.7 mm Inside TKR: 1515.5 x 1515.5 x 650 mm	1796 x1796 x 1045 1800 x 1800 at connector 1574 x 1574 x 204.7 1515.5 x 1515.5 x 650	Demonstrate
Mass	< 280 kg	270	Demonstrate
Power	< 31 Watts (conditioned)	14	Demonstrate
Instrument Lifetime	Minimum 5 yrs	> 5 yr.	Analysis

- You have already seen in ACD Overview presentation on how the two requirements in red need to be traded off against each other and how we came to a good balance between the two.

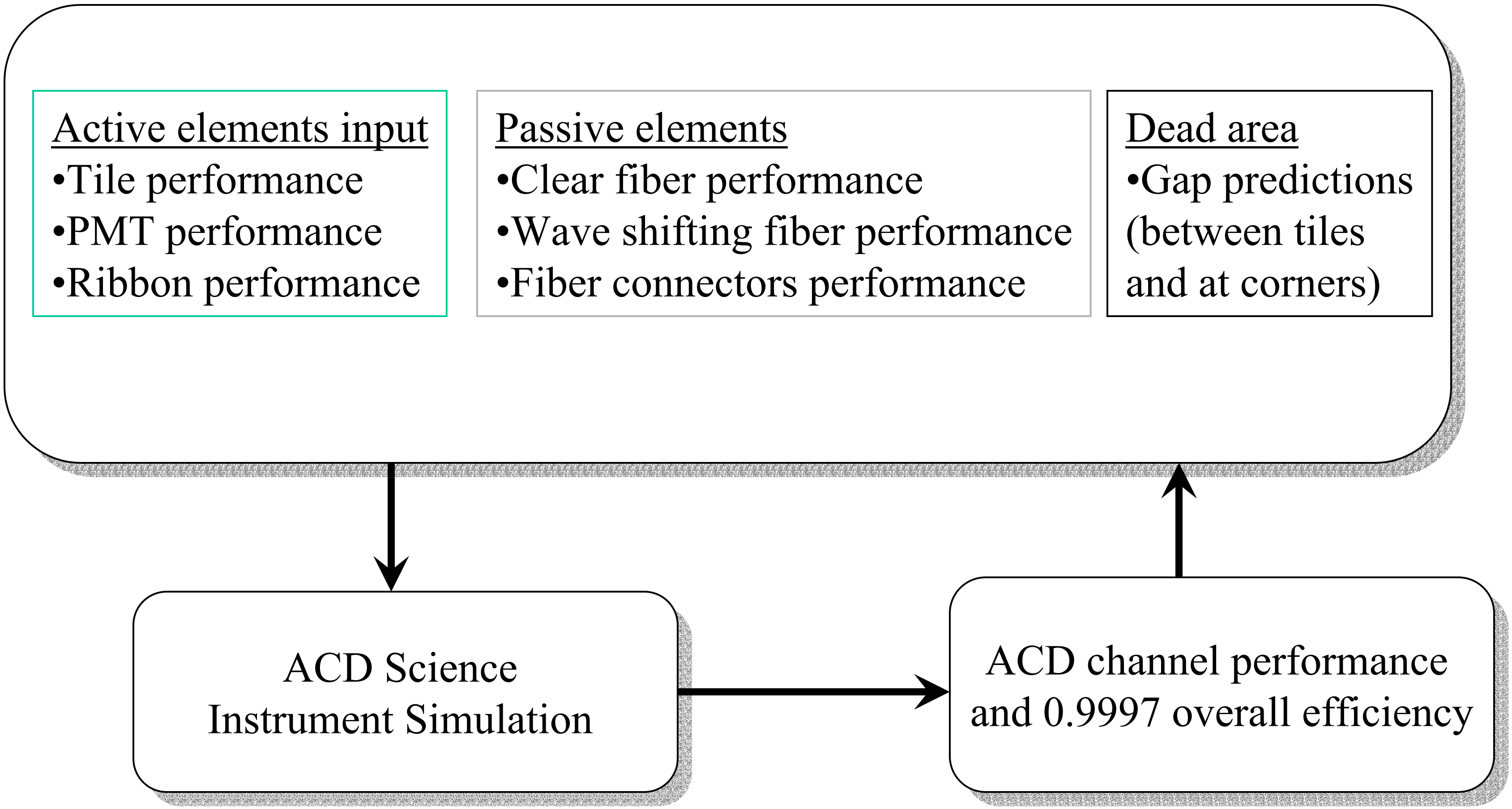
Level IV Requirements Outline

5.2 Charged Particle Detection
5.3 Adjustable Threshold on VETO Detection of Charged Particles
5.4 False VETO due to Electrical Noise
5.5 High-Threshold Detection
5.6 Adjustable High-Threshold
5.7 Level 1 Trigger Acknowledge (TACK)
5.8 Signals - (8 lower level requirements)
5.9 ACD Performance Monitoring - (10 lower level requirements)
5.10 High Voltage Bias Supply - (14 lower level requirements)
5.11 PMT - (6 lower level requirements)
5.12 Radiation Tolerance - (2 lower level requirements)
5.13 Reliability - (6 lower level requirements)
5.14 Commands - (10 lower level requirements)
5.15 Output Data Formats
5.16 Power Consumption
5.17 Total ACD Mass
5.18 Environmental Requirements - (11 lower level requirements)
5.19 Performance Life
5.20 Rate Requirement for Operation within Specification
5.21 Testability
5.22 Center of Mass
5.23 Volume
5.24 Instrument Coverage
5.25 LAT to ACD Gap.
5.26 Material interaction of gamma radiation (Gamma radiation due to ACD material interactions)
5.27 Thermal Blanket/ Micrometeoroid Shield Areal Mass Density
5.28 Gaps between scintillating tiles
5.29 Light Throughput

ACD Requirements

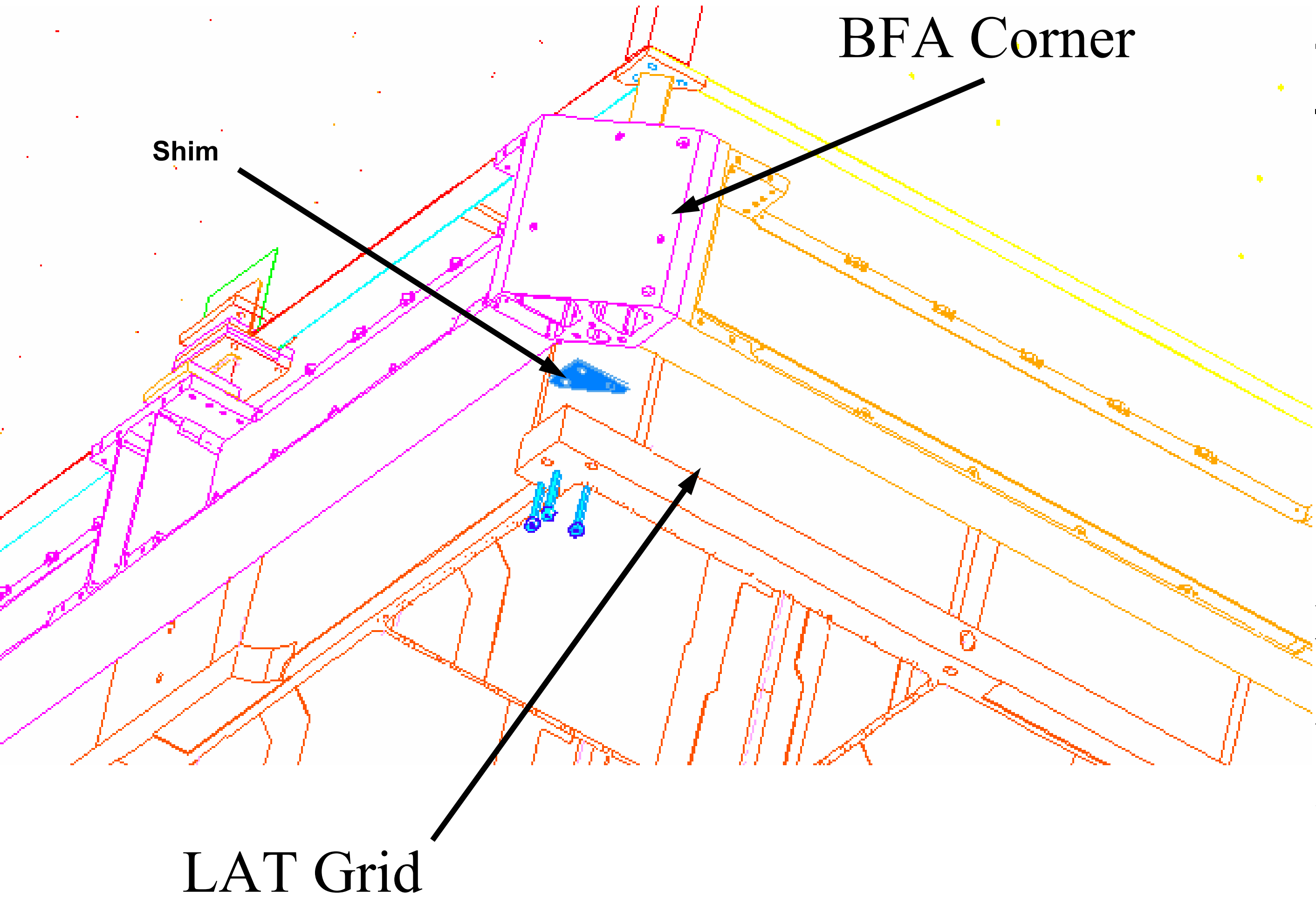
- Some important requirements flow through a science simulation

ACD Simulation Input Parameters



INTERFACES

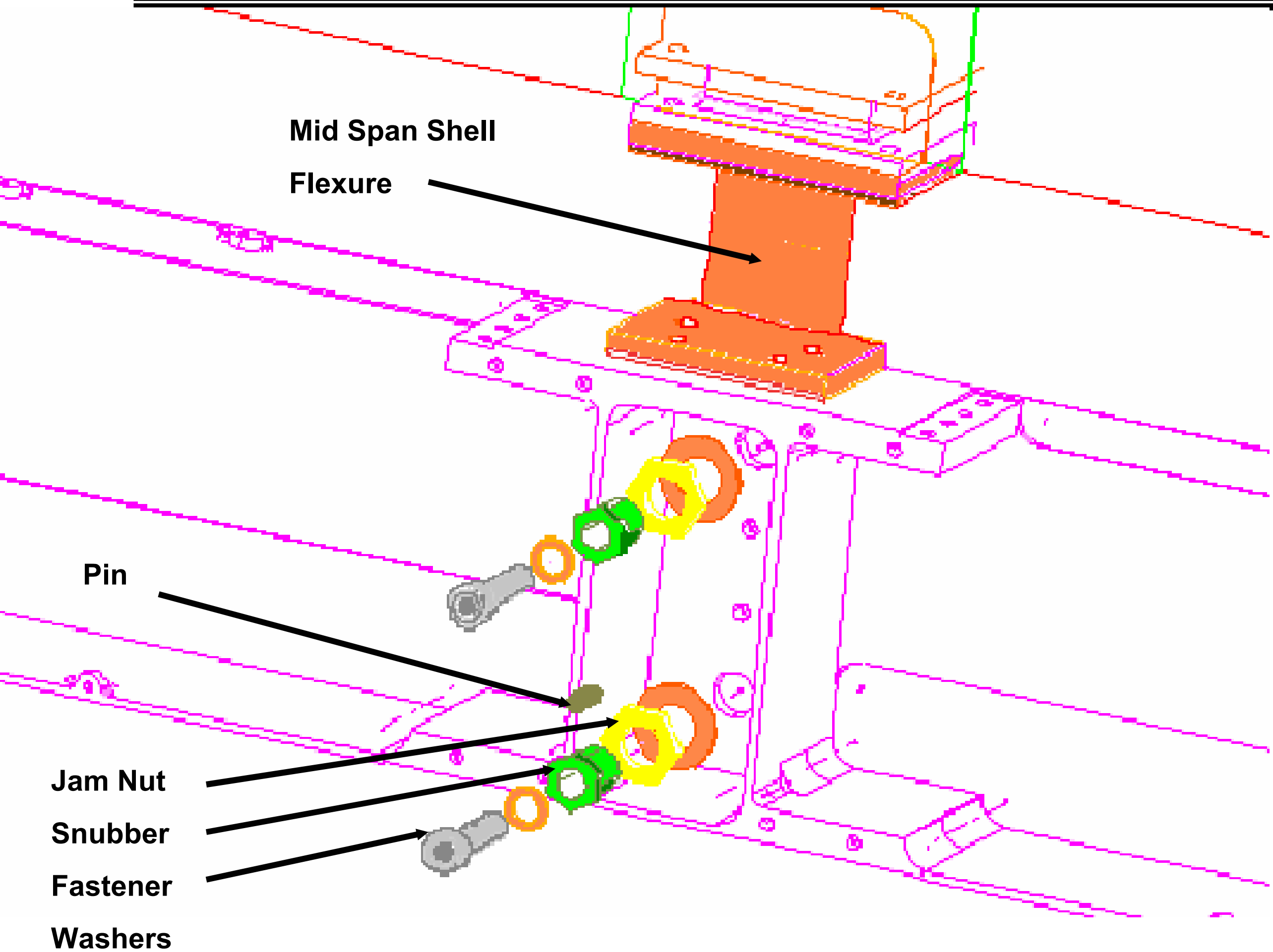
BFA Design



BFA connection to LAT Grid

- Connected in 4 corners, each with 3 fasteners and a shim.
- Registration to LAT Grid is planned via a pin and slot common to both the BFA and the LAT Grid.

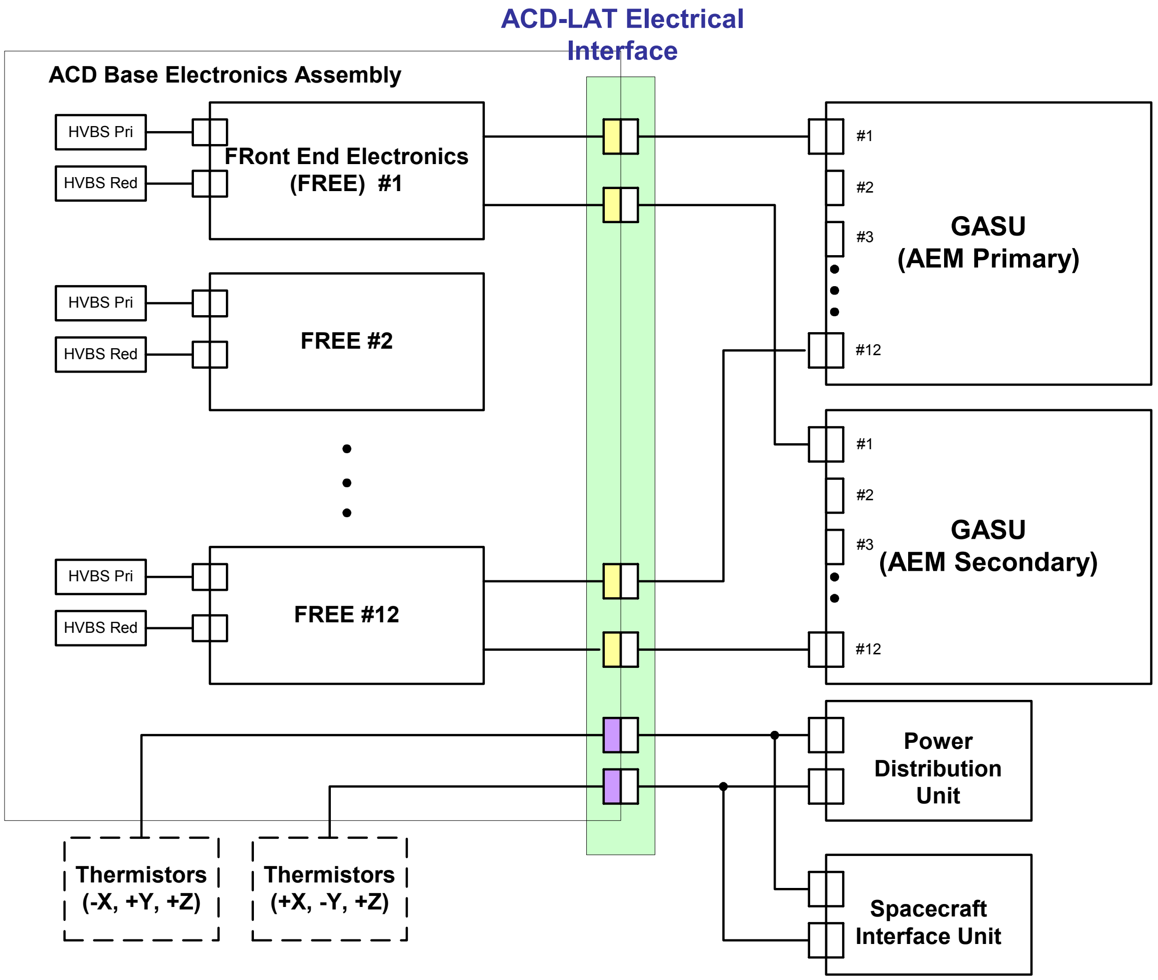
BFA Design



BFA connection to LAT Grid

- At each of 4 mid-span locations 2 fasteners and slip fit pin
- Gap Between ACD and LAT Grid is taken up with adjustable snubbers.
- Pin match drilled to LAT Grid after BFA is completed.
  - Pin is captured to accommodate slip fit.

Electrical Interface



- 24 identical robust circular connectors (38999, series 2) & 2 circular housekeeping connectors (38999, series 2)
- Parts, pin outs, signal def, grounding all defined in ICD

DATA PRODUCTS

(defined in Reqs. and specified in ICD)

- Channel specific charged particle VETOs
- VETO hit maps
- Pulse Height Analysis (PHA)
- Diagnostics
- Housekeeping (thermistor output, voltage monitor output, direct to AEM)

ACD Technical Budget Summary

Technical Resources –

- ACD Mass
  - Allocation 280 kg (raised 15% from ΔPDR)
  - ACD detailed estimate 270 kg
- ACD Power
  - Allocation 31 W (conditioned)
  - ACD detailed estimate 14 W max
- Thermal Interface (max dissipation across ACD-LAT interface)
  - Dissipation Allocation 16 W
  - Dissipation Estimate <14 W

Mass Summary

Item	Estimated Mass (Kg)	Calculated Mass (Kg)	Actual Mass (Kg)	Total Mass without Margin (Kg)
Mechanical Hardware				
Tile Shell Assembly (TSA)		29.8004		29.8004
Shell/Base Middle & Corner Flexures	1.6000	5.9824		7.5824
Base Frame Assembly (BFA)		25.1535	0.1248	25.2783
Tile Flexures	4.3900		5.0320	9.4220
Clear Fiber Cable & Fiber Ribbon Tiedowns	1.1840	0.1984	1.6800	3.0624
Shield/Blanket Attachments	0.4000		2.5840	2.9840
ACD/LAT Interface Hardware			0.6000	0.6000
Uralane & Safety Cable	1.0000			1.0000
			Mechanical Hardware Total	79.7295
Tile Detector Assemblies				
Tiles		95.3650		95.3650
Tile Wrapping		7.7700		7.7700
Tile Pig Tails & Clear Fiber Cables		8.5026	3.7896	12.2922
Fiber Ribbons	0.0000	1.3928		1.3928
Fiber Ribbon Wrapping		0.3472		0.3472
Fiber Ribbon Pig Tails	0.1600	0.1200	0.1712	0.4512
			Tile Detector Assemblies Total	117.6184
Electronic Hardware				
PMT Assemblies	0.2910		11.8340	12.1250
Chassis Structure		13.8360		13.8360
FREE Board & PCB		6.0360	0.0000	6.0360
HVBS		2.2560		2.2560
Power Distribution Board		1.7280		1.7280
Bulkhead Connectors & Brackets		2.2352	1.3000	3.5352
Harnessing, Tiedowns & Fasteners	0.5000		0.3120	0.8120
			Electronic Hardware Total	40.3282
Thermal Hardware				
Thermistors, Wiring & Tiedowns	2.3800			2.3800
Micrometeoroid/Thermal Blanket		30.0800		30.0800
			Thermal Hardware Total	32.4600
			TOTAL ACD	270.1361

Power Summary

		NOMINAL POWER CONFIGURATION					MAXIMUM POWER CONFIGURATION				
	No. Units Per Board	Total No. Units (Nom)	Nom. Current per unit	3.3V Current (Nom)	28 V Current (Nom)	Nominal Power	Total Number Units (Max)	Max Current per unit	3.3V Current (Max)	28 V Current (Max)	Max Power
Bus Voltage				3.30	28.00				3.60	29.00	
GAFE	18	216	0.0022	0.475	0.000	1.57	216	0.0022	0.475	0.000	1.57
ADC MAX145	18	216	0.0012	0.259	0.000	0.86	216	0.0012	0.259	0.000	0.93
GARC	1	12	0.0146	0.175	0.000	0.58	12	0.0146	0.175	0.000	0.63
LVDS Driver	20	240	0.0035	0.840	0.000	2.77	480	0.0035	1.680	0.000	6.05
LVDS Rcvr	6	72	0.001	0.072	0.000	0.24	72	0.001	0.072	0.000	0.26
HVBS (PMT Power)	1	12	0.0095	0.000	0.114	3.19	12	0.011	0.000	0.132	3.83
Cable Loss 2%				0.036	0.002	0.18			0.053	0.003	0.27
Power Totals						**9.39**					**13.54**

DESIGN DECISIONS

Design Decisions - R&D Testing

- **R&D Testing: Identify optimum design in terms of tile efficiency and light collection and map the response (light yield, efficiency) of a fiber/tile configuration in detail.**
  - Determine testing methodology and construct test configuration -complete
  - Determine optimum fiber spacing in tile –complete (LAT-TD-00438)
  - Determine optimum groove depth –complete (LAT-TD-00438)
  - Determine edge effects –complete (LAT-TD-00438)
  - Determine tile uniformity – complete (LAT-TD-00438)
  - Determine effects of fiber end treatments (Al'ized ends) – complete (LAT-TD-00438)
  - Determine fiber length effects –complete (LAT-TD-00438)
  - Determine MIP light yield in p.e.'s, and PMT gain requirements –complete (LAT-TD-00438)
  - Determine effects of broken fibers – complete (LAT-TD-00438)

- **Production Testing: Develop and implement test procedure and fixture to verify performance of every tile.**
  - Experience derived from R&D Testing will determine testing methodology and requirements
  - Tile Detector Assembly, Vibration, Thermal Vacuum and Performance tests completed (see ACD CM system)
  - Long tile and ribbon tests completed (LAT-TD-01239)

Design Decisions –Major Trades (since PDR)

- BEA repackaging to facilitate trouble shooting, access, and efficient spare approach
  - Went from FREE boards being vertically mounted one behind the other to a structural element to horizontally mounted Free boards, both accessible from the front, mounted to a removable chassis.
  - Complete, tested (including thermal vac cycles) spare chassis can replace a troubled chassis.

- Returned to two HVBS per FREE board (went to one in de-scope)

- Overall efficiency trade study
  - Detector channel study resulted in
    - Rerouting fibers to improve efficiency of channels with longest fibers
    - Re-mapping of PMTs to facilitate above rerouting and to reduce fiber crossings in areas with little volume.
    - Increase in the thickness of the top center row of detectors (longest fiber run to PMTs)
    - No better performing clear fiber options found
  - Gap analysis study
    - Structural load and thermal motions were analyzed to determine minimum gaps
    - Vibration tests on some gap scenarios were run
    - Third fiber row was added to scintillator ribbons.
    - Some tile sizes modified to increase overlap

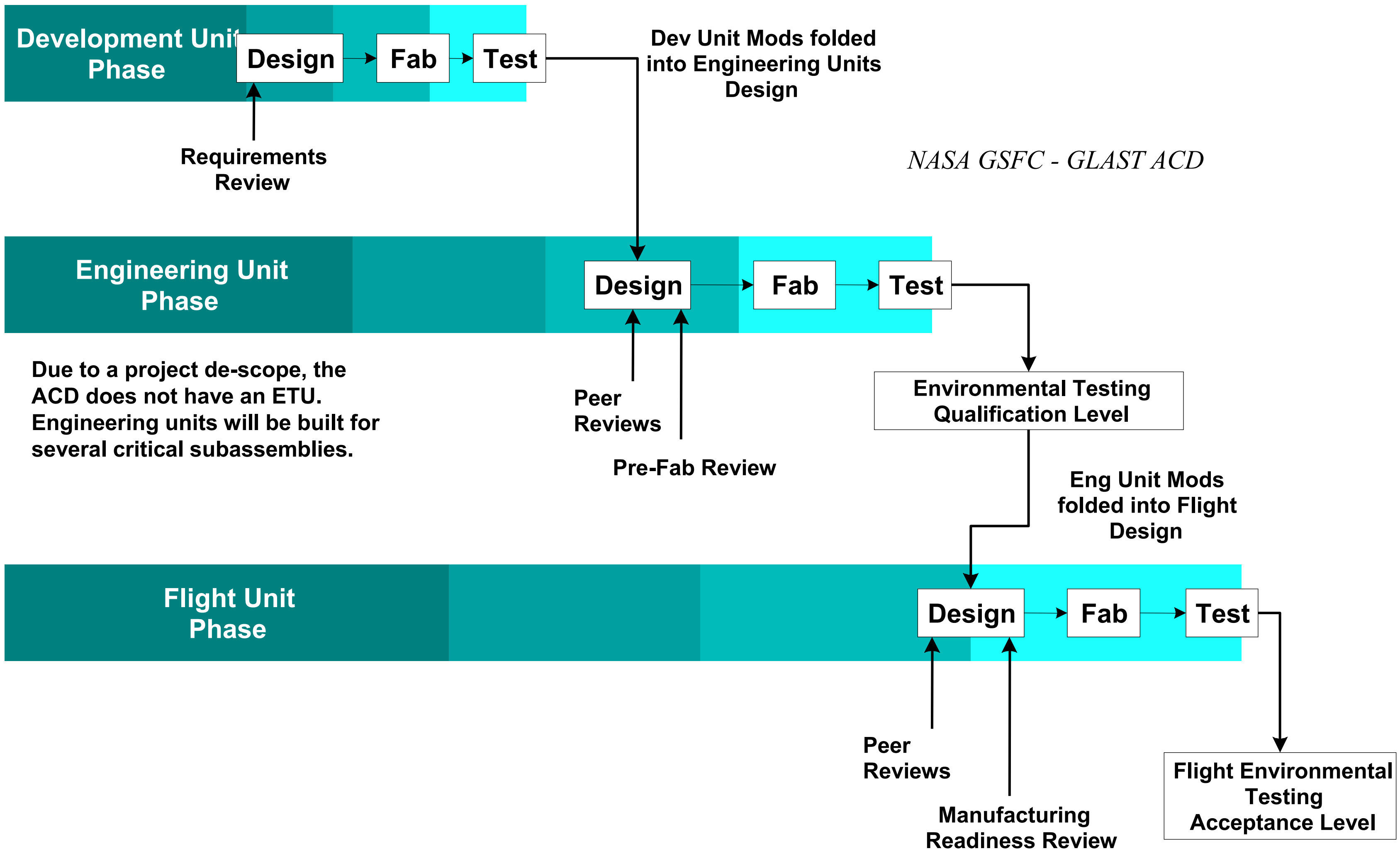
- Analog ASIC design approach and testing scenario changed (modified the design and brought in additional outside expertise)

- Micrometeoroid design change approach (additional spacer vs additional layers to accommodate reduced performance prediction from new analysis model)

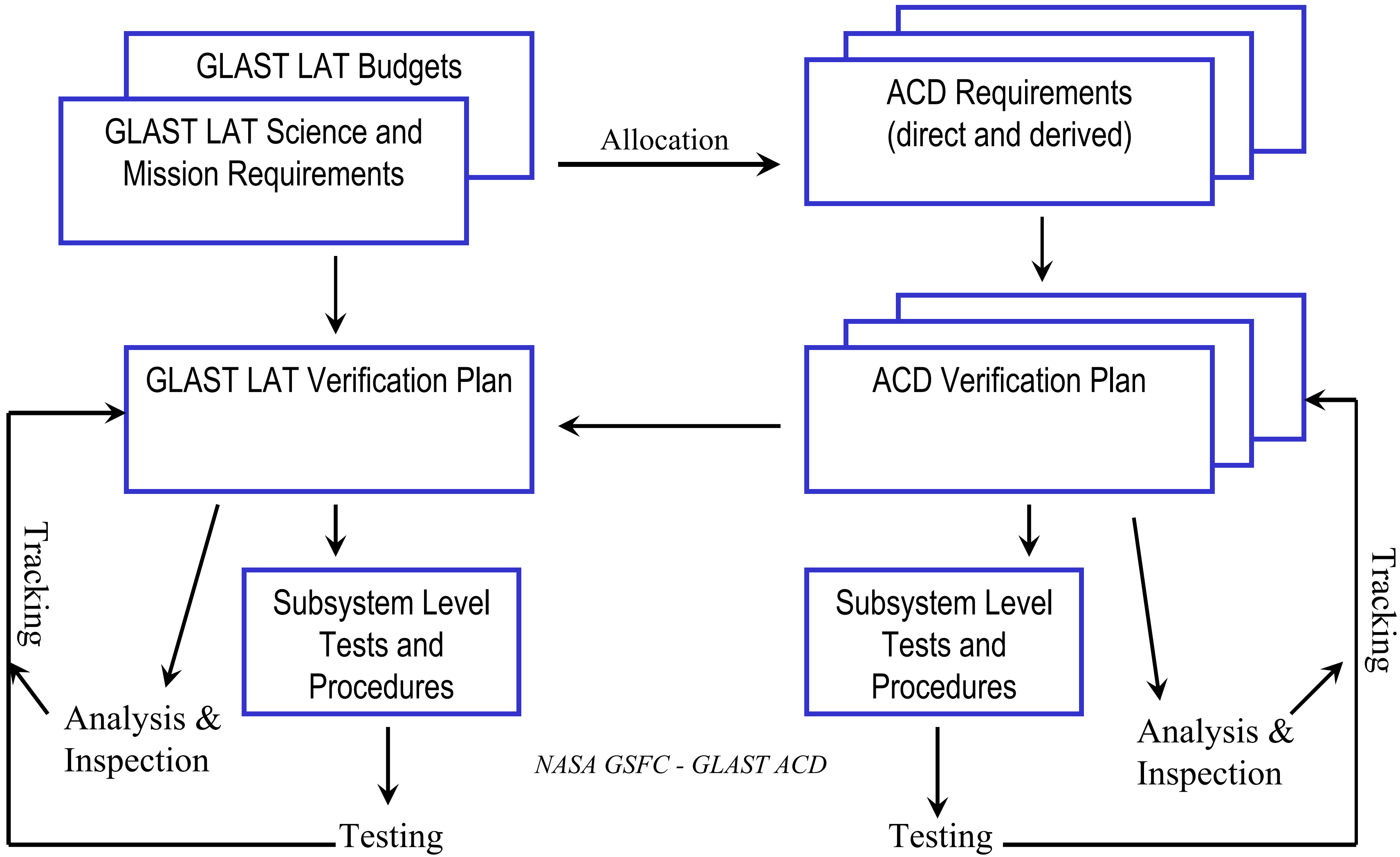
- Smaller changes – Added two instrumentation connectors, changed connector type to lower profile connector, lower tile design modifications

VERIFICATION

ProtoFlight Development Flow



ACD Requirements and Verification Tracking



ACD Verification Database

- ACD has created a Verification database in DOORS linked to the Requirements Database to Track Verification (Verification Plan - ACD-PLAN-000050)

ACD Verification Tracking Database

LAT ACD Subsystem Level IV Requirements and Verification Table, LAT-SS-00352	Verification Method	Verification Procedure	Verification Stage/Status	Verification Rationale/Comment	Verification Action	1st tim
5.2 Charged Particle Detection						
The ACD shall produce both fast and slow VETO signals in response to PMT signals resulting from charged particles traversing the ACD tiles and ribbons.	Test	ACD Comprehensive Performance Test (CPT) (ACD-PLAN-000038)	Not Started	Muons test		
5.3 Adjustable Threshold on VETO Detection of Charged Particles						
The threshold for detecting charged particles shall be adjustable from 0.064 to 1.28 pC (0.1 to 2 MIP), with a step size of ≤0.032 pC (0.05 MIP).	Test	ACD CPT (ACD-PLAN-000038) FREE Functional Test (ACD-TBD-XX)	Not Started	The FREE Functional will characterize the adjustable threshold to the spec step size. The CPT will test this adjustabililty with the TCI circuit, however, it currently doesn't have the resolution to fully test this function.		
5.4 False VETO due to Electrical Noise						
The total ACD false VETO trigger rate due to noise shall be less than 10 kHz (~46Hz per channel) at 0.096 pC (0.15 MIP) threshold (assuming 1 us VETO pulses).	Analysis Test Simulation	ACD CPT (ACD-PLAN-000038)	Development	Set threshold to 0.15 MIP and then reduce HVBS output until VETO count rate no longer decreases. The resulting VETO rate is the false trigger rate due to noise.		
5.5 High-Threshold Detection						
The ACD shall detect pulses due to highly ionizing particles, carbon	Test	ACD CPT (ACD-PLAN	Development	200 to 1000 MIP will be		

Links between Requirements

ACD Level III and IV Requirements Database

ACD-LAT ICD Requirements and Verification Database

ACD Allocation Tables

ACD Test Databases

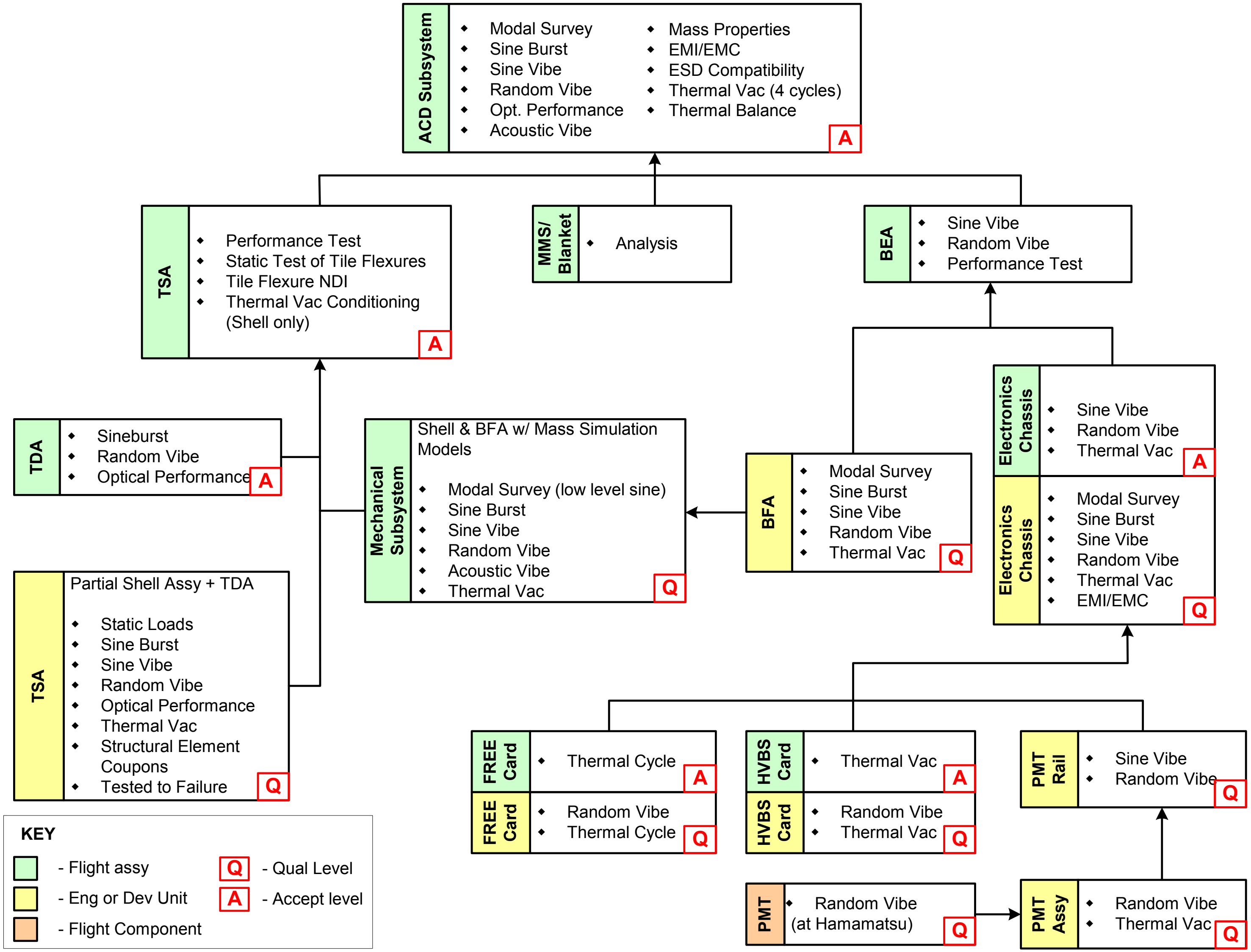
Test Matrix

Item	Level of Assembly	Unit Type	Supplier	Test Levels	Test Status	Modal Survey (low level sine survey)	Static Loads	Sine Burst	Sine Vibration	Random Vibration	Mechanical Function	Performance Testing (Optical)	Acoustics	Mass Properties	Interface Verif.	EMC/EMI	ESD Compatibility (Grounding)???	Magnetics	Screening Process	Aliveness (A) / Functional (F) / Comprehensive (C)	Thermal-Vacuum Cycle	Thermal Cycle	Thermal Balance	Remarks
	Hardware			Structural/Mechanical											Electrical						Thermal			
ACD Subsystem (Integrated ACD)	**S**	**F**	**GSFC**	**Acpt**		**X**		**X**	**X**	**X?-r**		**X**	**X**	**X**	**X**	**X**	**X**			**C**	**4**		**X**	**Acceptance Levels**
Tile Shell Assembly	SA	F	GSFC	Acpt										X ?										
Tile Shell Assembly - partial	SA	D	GSFC	Qual			X-b	X	X	X	X			X							6			
ACD Mechanical Subsystem (no elect or Det)	S	F	GSFC	Qual		X-e		X-e	X-e	X-e	X			X							2			ACD Structure w/mass sims, no elect or det
Shell	C	F	TBD	Par Qual		X-e		X-e	X-e	X-e				X							2 ?			
Shell - partial	P	D	GSFC	Qual			X-b	h	h	h														
Tile Detector Assembly	SA	F	Fermilab	Acpt				X		X		X-d	h	X						A, F-h				117 Flt TDAs
Tile Detector Assembly	SA	S	Fermilab	Acpt						X		X-d									8			28 Flight Spares
Tile Detector Assembly	SA	EM	Fermilab	Qual				X	X	X		X-d		X						F	6			20 TDAs
Tile Detector Assembly	SA	D	Fermilab	Qual			X	X		X		X-d									6			Functional testing code660
TDA Tiedown (Flexure)	P	F	GSFC	TBD			X-c							X										Test bonded joint
TDA Tiedown (Flexure) ?	P	EM	GSFC	Par Qual			X-c	X	X	X	X			X							h			Test bonded joint
TDA Tiedown (Flexure)	P	D	GSFC	Qual			X-b														h			Characterize flexures
WSF/Clear Fiber Connector	C	F	GSFC	TBD										X						A, F-h				
WSF/Clear Fiber Connector	C	EM	GSFC	Par Qual						h	X	X-c		X						F	h			
WSF/Clear Fiber Connector	C	D	GSFC	Qual				X ?		h	X	X-d								A?	h	8-d		Several development models
Base Frame	C	F	GSFC	Par Qual		X-e-c		X-e-c	X-e-c	X-e-c				X							4-c			
Partial BFA & Electronics Chassis	SA	EM	GSFC	Qual		X		X-?	X	X						X	X?	X?		F		2?		Corner or one side BFA, BEA assemb
Base Frame - partial	C	D	GSFC	Par Qual			X		X-e	X-e														
Shield & Thermal Blanket	C	F	GSFC											X							4-c			Similarity to dev. model
Shield & Thermal Blanket	C	EM	GSFC											X										Similarity to dev. model
Shield & Thermal Blanket	C	D	JSC, GSI	Qual																	6			Characterize thermal perf., particle impact
Clear fiber cable assembly	SA	F	GSFC	Qual					X-c	X-c		X								A				
PMT/Fiber Connector	C	F	GSFC	TBD						X-c	X-c	X-c		X						A				
PMT/Fiber Connector	C	EM	GSFC	Par Qual							X	X-c		X						F	6-c			
PMT/Fiber Connector	C	D	GSFC	Qual						X	X	X-d								F		8-d		Several development models
Base Electronics Assembly	S	F	GSFC	Acpt					X	X										F				
Electronics Chassis	SA	F	GSFC	Acpt					X	X				X	X					F	2?			(FREE, HVBS, PMT)
Electronics Chassis	SA	EM	GSFC	Qual		X		X	X	X				X						F	10			(FREE, HVBS, PMT)
Electronics Chassis	SA	D	GSFC	Qual																F	2			(FREE, HVBS, PMT)
Electronics Chassis (FREE, HVBS, PMT)	SA	BB	GSFC																	F				parts

Test Matrix

	Hardware			Structural/Mechanical											Electrical						Thermal			
Item	Level of Assembly	Unit Type	Supplier	Test Levels	Test Status	Modal Survey (low level sine survey)	Static Loads	Sine Burst	Sine Vibration	Random Vibration	Mechanical Function	Performance Testing (Optical)	Acoustics	Mass Properties	Interface Verif.	EMC/EMI	ESD Compatibility (Grounding)???	Magnetics	Screening Process	Aliveness (A) / Functional (F) / Comprehensive (C)	Thermal-Vacuum Cycle	Thermal Cycle	Thermal Balance	Remarks
FREE Board (12)	C	F	GSFC	Acpt					X-c	X-c					X					F	2			12 Units
FREE Board (2)	C	S	GSFC	Acpt						X					X					F	12 ?			2 Units, therm cycle enough to use late
FREE Board (4)	C	EM	GSFC	Qual		h		h	h	X				X	X	h	?			F	2			2 Units, possibly tested in partial frame?
FREE Board (4)	C	D	GSFC	Par Qual											X					F				4-6 Units
FREE Board (2)	C	BB	GSFC																	F				
FREE Board Parts (refer to Parts Plan, See n	P	F,D	Multiple	*																				Using NASA approved flight parts, see note
PMT Rail	SA	S	GSFC	Acpt					X	X														
PMT Rail	SA	D	GSFC	Qual					X	X														
PMT Subassembly (194)	P	F	H, GSFC	Acpt						X-c					X					F		X ?		
PMT Subassembly (46)	P	S	H, GSFC	Acpt						X					X					F	12 ?			
PMT Subassembly (qual PMTs)	P	EM	H, GSFC	Qual		h		h	h	X				X	X	h	?			F	2			
PMT Subassembly (6)	P	D	H, GSFC	Par Qual			X-b			X					X					F	6			
PMT Subassembly (30)	P	C	H, GSFC												X					F		X		
PMTs (not bonded) (240)	P	F	H			h		h	h	h		h							X	F-s				
PMTs (not bonded) (10)	P	D	H							X ?		X							X	F-s				
PMTs (not bonded) (30)	P	C	H																	?				
Resistor Network (194)	C	F	GSFC							h										F				
Resistor Network (46)	C	S	GSFC							h										F				
Resistor Network (calibration)	C	EM	GSFC							h				X	X					F				
Resistor Network (6)	C	D	GSFC												X					F				
Resistor Network (46)	C	C	GSFC																	F				
HVBS (24)	C	F	GSFC	Acpt					X-c	X-c					X					F	2			24 Units
HVBS (2)	C	S	GSFC	Acpt					X	X					X					F	12 ?			2 Units, therm cycle enough to use late. Spares tested first and only one acceptance tested separately.
HVBS (4)	C	EM	GSFC	Qual		h		h	h	X					X	h	?			F	2			4 Units
HVBS (3)	C	D	GSFC	Par Qual																F				3 Units

Top Level Environmental Test Flow (from matrix)



RISK (Briefly)

Risk

- If failures occur, ACD is designed to fail 'gracefully', major failures result in incremental steps in performance. Other than a major micrometeoroid hit, it takes multiple failures to fail a detector channel. Complete detector channel failures leave holes in coverage.
- Micrometeoroid shield penetration is the only in orbit single point failure risk. ACD fails to meet the efficiency requirement with one tile destroyed by micrometeoroid penetration.
- A GARC failure results in loss of 18 PMTs leaving 18 detector tiles operating on one PMT, marginally meets efficiency requirement.
- The only other way to lose a entire detector tile is for multiple failures of other components.
- Each Detector tile has fibers leading to two separate PMTs on separate electronic chassis. PMTs are powered by separate HVBSs.
- Each electronic chassis has redundant HVBSs.
- PMTs can be adjusted in orbit to counteract degradation.
- New micrometeoroid shield orbit debris predictions resulted in reduction in predicted performance. Design being modified to increase performance.

Risk

- As part of the reliability/ risk program, the following additional activities have been performed in preparation for CDR:
  - Failure Modes and Effect Analysis and Critical Items List ACD-RPT-000042 *(LAT-TD-00913)*
  - Limited-Life Item Analysis (LAT-TD-00523)
  - Reliability Assessments and Worse Case Analysis (ACD-RPT-000071)
  - Fault Tree (ACD-RPT-000072)
  - Parts Stress and De-rating Analysis
  - Continuous Risk Management Plan (LAT-MD-000067)
- Refer to Safety & Mission Assurance presentation for key results.

ACD Development Risks and Mitigations

(LAT-MD-000067)

LAT Risk Identification & Mitigation Database	ACD Subsystem Risk Items						
Phase	Risk Description	Probability	Cost Impact	Schedule Impact	Technical Impact without mitigation/ Description	Mitigation Plan/Results	Contigency Plan
Risk in Design, Assembly, and Verification Phase	Design flaw in flight ASIC	Moderate	Moderate	Moderate to High	2 - lose effective area, lower background rejection, no diffuse measurement	Three foundry runs, comprehensive test program, and peer reviews	Replace with newly designed ASICs
	Tile Assy. (Tiles, ribbons & PMT) fail efficiency parameter test in ACD Qualification	Low	Moderate	Moderate to High	2R - Lose ability to measure diffuse radiation	Early testing, detailed simulations	Thicker tiles
	Corona in Thermal Vac around HV	Low	Moderate	Moderate to High	2 - if systematic, lose effective area, lower background rejection, no diffuse measurement 3 - Lower efficiency if workmanship failure	Early testing and qualification of subassembly	Analyze and redesign the PMT assembly process for systematic failure. Re-pot PMT assembly for workmanship failure.
	PMT Fails in test	Low	Low	Moderate	3 - Lower efficiency	PMT qualification program and burn-in	Replace with spares
	Light Leak in the detector system channel	Moderate	Low	Moderate	2R - Lose ability to measure diffuse radiation	Early testing and qualification of subassembly, handling procedures	Additional 'light wrap' can also be added
	Mechanical interference found during assembly	Very Low	Low	Moderate	1 - cannot deliver ACD	Design checks and early Fit checks	Modify Parts
	Waveshifting fibers break in environmental testing	Low	Low	Moderate to High	3 - Lower efficiency	Subassembly test, careful tiedown. If you had a failure in a later environmental test, the cost will increase.	Re-design the fiber cable tie-downs, change fiber manufacturer
	Tile comes loose in acoustics	Low	Low	Moderate	3 - Lower efficiency	Conservative design, analysis, mechanical qualification program	Analyze failure, repair or redesign
	EMI/EMC produces noisy signals	Low	Low	Low	3 - Lower efficiency	Careful design, early subassembly tests	Add shielding and Grounding etc as needed
	HVBS fails in test	Low	Low	Low	2R - Lose ability to measure diffuse radiation	HVBS qualification program and burn-in	Replace with spares or modify design
	Structural Failure (I.e. laminate failure, bond failure, etc)	Low	Low	Low to Moderate	3 - Lower efficiency	analysis, mech. qual program	Analyze failure, repair or redesign
	Other BEA electronics subassembly failure	Low	Low	Moderate	2R	Early testing and qualification of subassembly	Replace with spares
	QA finds problem in part (ie GIDEP alert)	Very Low	Low	Low to Moderate	3 - Lower efficiency	None	Replace w/ different part
	Civil Servant test conductors pulled off for another project	Moderate	Moderate	Moderate	N/A	High visibility with GSFC management	Hire and Train test conductors

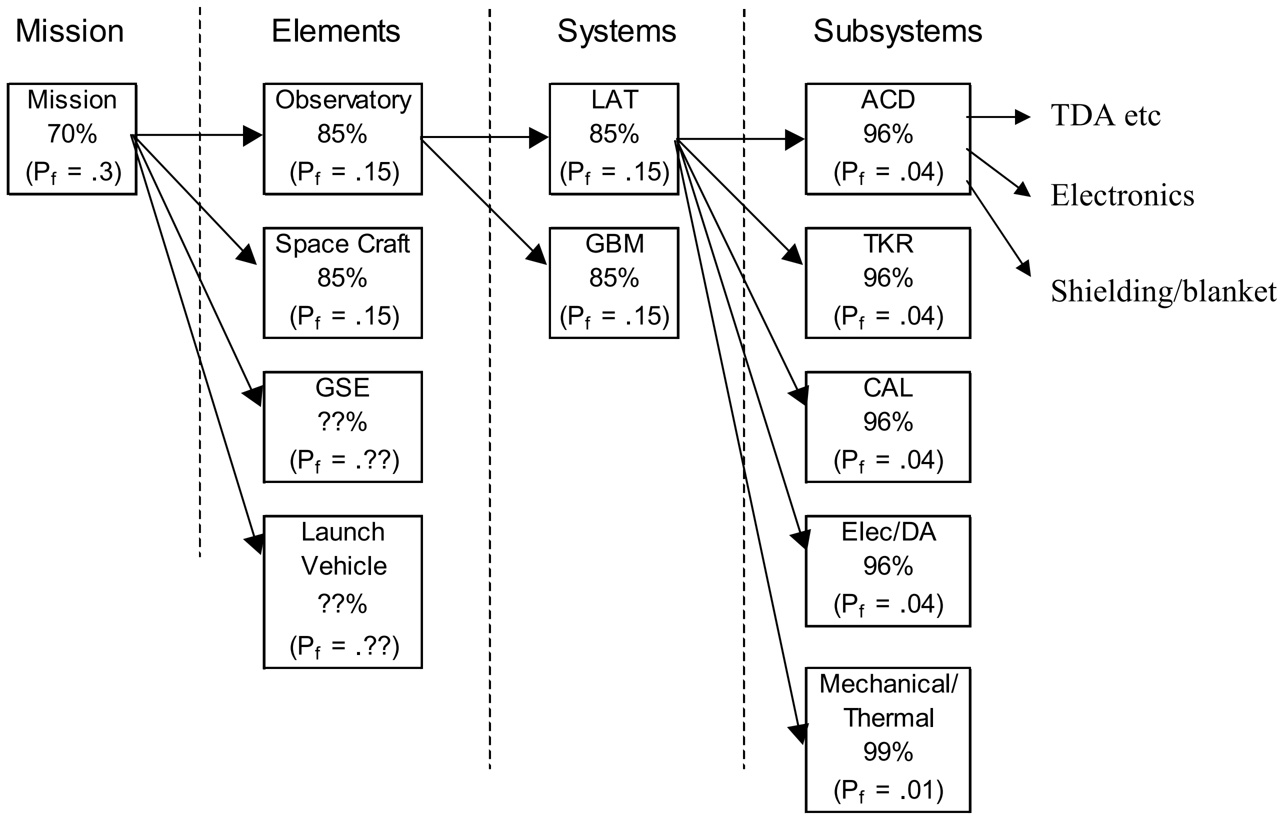
ACD Flight Risks and Mitigations (LAT-MD-000067)

LAT Risk Identification & Mitigation Database			ACD Subsystem Risk Items				
Risk in LAT or Observatory I&T	Mechanical Interface problem between ACD and LAT Grid	Very Low	Low to Mod	Moderate	1 - cannot fly without ACD or something above tracker	Clearly defined ICD, design checks and early Fit checks	Analyze and fix incompatability
	Electrical Interface problem between ACD and LAT AEM	Low	Moderate	Moderate to High	2- May lose some capabilities depending on incompatibility	Clearly defined ICD, qualification testing with AEM flight like EGSE	Analyze and fix incompatability
	Electronics component/subassembly fails	Very Low	Low	Low	3 - Lower efficiency	Early testing and qualification of subassembly, ACD subsystem verification testing.	Plan an adequate spares program to replace damaged electronics assembly
	Damage to tile detector assembly (tiles, ribbons & PMT)	Very Low	Low	Moderate	3 - Lower efficiency	Trained personel and proper procedures for anyone operating on LAT instrument.	Plan an adequate spares program to replace damaged portion of the tile system. Damage to 'light wraps' can probably be repaired.
	Damage to composite structure	Very Low	Low	Moderate	3 - Inadequate strength	Trained personel and proper procedures for anyone operating on LAT instrument.	Fix the damage portion of structure
	QA finds problem in part (ie GIDEP alert)	Very Low	Low to Moderate	Low to Moderate	3 - Lower efficiency	None	Replace with different part
Risk in Flight	Damage to tile detector assembly (tiles, ribbons)	Low	N/A	N/A	3 - Lower efficiency	Analyze micrometeoroid environment (most likely source of penetration). Design and Test shield.	Operate with lower efficiency, while still meeting minimum science requirements
	Degradation of PMT performance (gain) or PMT Failure	Moderate	N/A	N/A	3 - Lower efficiency	Design in HVBS adjustability for PMT gain degradation. Test qualification program for PMTs.	Operate with lower efficiency, while still meeting minimum science requirements
	HVBS Failure	Low	N/A	N/A	2R - Lower efficiency	Add redundant HVBS	Switch to redundant HVBS
	Thermal Blanket Damage	Very Low	N/A	N/A	3 - Lower efficiency	Analyze blanket attachments, Blanket and ACD handling procedures, maintain some margin in thermal analysis predictions	Operate with lower efficiency.
	Other Electronics Failure	Very Low	N/A	N/A	2 - lose effective area, lower background rejection, no diffuse measurement	Test qualificaiton program for all electronics.	Operate with lower efficiency, while still meeting minimum science requirements

RISK

Redundancy

Reliability Allocation



<u>Reliability</u> - is defined as the probability of successfully meeting mission objectives at end of life. P_f is probability of failure.

TECHNICAL ISSUES

Technical Issues and Status

Technical Issues and Requirement Non-compliance *

- **Electronics Chassis Packaging – Progress continues to be made on finalizing BEA electro-mechanical packaging design.**
  STATUS and RESOLUTION - Structure design/analysis is fairly complete, some tweaks due to analysis have just been completed. May relax some tight fits on harness to reduce assembly risk. Had to wait for side stay clear growth sign off to consider this. See issue below.

- **Potential BEA connector side stay clear violation (ICD/IDD, Level III, 5.22) – LAT Connectors could, depending on tolerance stack up, extend slightly into stay clear.**
  STATUS and RESOLUTION - Changed to lower profile connector and pushed connector rear harness dimensions down. Design now fits into old stay clear with no margin. LAT pursued 1cm expansion of side stay clear with spacecraft vendor and project office. Agreed to by all parties and now reflected in version of IDD currently in sign off. This will allow for margin, relaxation of tight fits and potential expansion of harness size based on engineering model results. Stay clear issue is Fully Resolved.

- **Analog ASIC design * (see electrical presentation) - We have caught a variety of problems in the analog ASIC design. Some functions were not working. Design has been updated.**
  STATUS and RESOLUTION –We have solved most of the problems and modified the design for latest fab runs. We have received additional SLAC expertise and asked for some GSFC expertise to help with final design updates and more importantly to help us test for future ones in a more reliable way.

- **5 Year Reliability * (Level III 5.13, 5.14 & 5.4), Our overall 5 year reliability calculations show we are slightly below meeting our Level III efficiency requirement (.92 to .95 vs the .96 req). Other reqs are met at .96 reliability or better.**
  STATUS and RESOLUTION We are revisiting provided numbers and internal margins. We are marginal only in meeting the efficiency req for 5 years, not other requirements. The reliability requirement flow down may have to be reviewed at the GLAST project level.

Technical Issues and Status

Technical Issues and Requirement Non-compliance *

The next two issues involve components that go into determining if we meet our overall efficiency requirements. Changes in these areas had to go through the ACD Instrument science simulation code to see their combined effect on the overall efficiency

- **Long Fibers/Efficiency Issue (Level III, 5.4) – The length of some fibers were long, combined with fibers not quite performing as advertised, caused light yield at PMT to not meet requirement for some channels.**

  STATUS and RESOLUTION –Re-mapped the detector to PMT locations, which allowed us to shorten our optical fiber lengths, has been forwarded to LAT which has agreed to change which is reflected in updated ICD currently in signature cycle. Mechanical optimization also complete. Primarily we re-routed the fibers from the outside top and second row tiles on the X side around the corner to FREE cards on the Y side, This change alone has brought our problem side detectors into compliance with individual channel efficiency requirements they needed to meet our overall efficiency requirement. We have also increased the thickness of the top center row tiles to 1.2 cm to improve their performance. Fully resolved.

- **Tile Gap/Efficiency Issue * (Level III, 5.4) – The gaps that are needed between tiles reduce the ACD efficiency. The size of gaps are driven by thermal expansion/contraction, tile vibration, and tolerances.**

  STATUS and RESOLUTION -Several solutions particular to certain gaps have been decided on. Acoustic analysis and TDA test results have provided updated minimum gaps which are run through the simulations to update efficiency. The smaller gaps provided in the update make in unlikely additional steps will be needed (for example a reduction on the survival test high temp spec). Will be resolved when simulation results (expected this week) show ACD meets eff. req. with new gaps (which we expect them to show) and those gaps are fully represented in CAD design

Technical Issues and Status

Technical Issues and Requirement Non-compliance *

- **Micrometeoroid shield, (Level IV Req 5.13.5, 5.18.11) – Reduced performance prediction from new analysis model. Related issue, LAT has recently informed us *updates* to the environment for debris, Micro-meteoroid and Atomic Oxygen has not yet been 'officially' defined for the LAT by the project office.**

  STATUS and RESOLUTION - Redesign is in progress which will solve this. (we will have to track the updates in official req flow down before actual implementation)

- **Light leaks in TDA and PMT assembly * (Level III, 5.3, 5.2) – Light leak test revealed small light leaks in a bread board TDA.**

  STATUS and RESOLUTION - Fixes to leaks at PMT have been proposed and agreed to. Minor changes in sealing and taping at connector interfaces and tile will be tested for effectiveness. TDA Handling procedure is being created to prevent small punctures.

- **Other issues –Development unit PMT failure , we had a development PMT fail after assembly. Evidence points to vac leak. Failure Review Board is currently has created and has implemented a plan to determine exact failure cause. IDD clarifications – IDD still has some tolerance and dimensioning approach clarifications we are working on for the next version. Some 'growing pains' for being first LAT subsystem through CDR/Peer Review. Some LAT controlled interface documents have had slow update cycles. Tile mount design mechanical peer review input – Lower tile mount slip stick design and angle mount of flexures not yet verified by test.**

- **Other recently resolved Non compliance Issues – Mass (Level III, 5.19) allocation increased from delta PDR level, Attenuation (Level IV 5.26) calculation updated shows we meet 6% requirement**

SUMMARY

- Accounting and tracking of requirements is well defined.
- Requirements flow and relationships are well defined.
- We have showed our major system interfaces.
- Systems and interface documentation is signed off in the CM system or has entered that final process.
- We have discussed our development test work and major trade studies since PDR.
- Our verification approach and tracking is clearly delineated and documented.
- Major risks and risk mitigations are understood.
- A limited number of technical issues must be resolved before the manufacturing readiness reviews in those areas.
- Approaches to addressing those issues are clearly identified.

Backup

Current Issues and Status

9/26/02 – Notes from Performance Improvement Meeting. Changes agreed on are in BOLD BLUE.

Topic	Discussion	Proposed Solution
Improve scintillating fiber ribbons	If we can improve the efficiency of the ribbons, they help seal the gaps better. This change has minimal impact.	**Reconfigure ribbons from two layers to three layers**.
Vertical gaps (Ken's Case 3)	Launch loads drive the vertical gaps (between overlapping tiles) larger than planned. This opens paths for particles to penetrate with no signal.	**Increase tile size by 1 cm in the overlap direction**. This covers the increased vertical gaps. **Use Ken's calculated 2.4 mm vertical gaps**.
Side-by-side gaps (Ken's Case 1)	Looked like a problem for -45 C, but those temperatures seem unlikely now. If we can reduce the gap slightly, we should be OK at -20 C, which can probably be achieved with change in thermal design.	**Reduce scintillator gap to 2 mm at room temperature,** assuming that we can take up part of the thermal expansion and mechanical tolerances with the soft wrapping materials. **Reduce MLI emittance to 0.03 or less** Increase tracker emittance.
Perpendicular gaps (Ken's Cases 2)	These gaps are driven by the launch loads, especially acoustics. The original analysis was considered not stringent enough and the GEVS loads were thought to be too extreme. A full acoustics analysis is in progress.	Assume the GEVS loads and do the analysis and design. Consider the gaps at room temperature, not at 45 C. **Reduce the calculated gaps by 0.5 mm**, test for damage from having the wrapping materials touch during vibration (they are soft, but strong). Re-evaluate after the TDT and acoustics analysis.
Perpendicular gaps at corners (Ken's Cases 2a and 2c)	Case 2b seems not to be a problem, because the ACD "crown" reduces the chance of any particle reaching the tracker through the gap. The corners were already a concern because the edges of the tiles have lower efficiency (and a corner puts two low-efficiency regions together). In the BFEM and in Alex'	**Increase the tile sizes by 5 mm** to give more complete overlap at the corners. This may require notches in the tiles for the overlaps.

Partial detector Gaps table from last month for reference