

DRAFT: Trigger Primitives from the ACD Box

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The purpose of this note is to define the trigger primitives that will be produced in the ACD electronics box. The goal is to reduce the number of interface wires between the ACD electronics and the “Trigger electronics cards/box”.

Define the three thresholds as follows:

Low level threshold (0.1 +/- 0.05 MIP)

– LLD (aka ZS for zero suppress) – To activate ACD

Veto threshold (0.3 +/- 0.1 MIP)

– VETO (aka LO – for use in VETOing background

High level threshold (25 +/- 5 MIP)

– HLD (aka HI or CNO) – for keeping heavy nuclei carbon and above

List below is independent of redundancy considerations that may dictate these lines are all “doubled up”. (N.B. The set of tiles that goes into any of these triggers can be adjusted in flight.)

I. These three (3) lines are for use in L1 trigger veto:

- 1.) “OR” of all (not including bottom two rows) tile VETOs – any single tile triggers this line (65 inputs to each of two redundant circuits).
- 2.) “OR” of all (not including bottom two rows) tile VETOs – any two tiles trigger this line (same 65 inputs to each of two redundant circuits as 1 above).
- 3.) “OR” of all (not including bottom two rows) tile VETOs – any “three or more tiles” trigger this line (same 65 inputs to each of two redundant circuits as 1 above).

II. There are sixteen (16) supertiles to form veto’s to be used at L1 at a tower level.

- 4.) “ORs” of “supertile set” to form VETOs for each tower (same 65 inputs to each of two redundant circuits as 1 above, ‘OR’ of subsets as follows: corner towers – 12 inputs; side middle towers – 8 inputs; middle 4 towers – either 4 or 16, plan for 16).

III. These two (2) lines are for use in selecting events for calorimeter calibration:

- 5.) “OR” of all tile HLDs for all top tiles (25 inputs).
- 6.) “OR” of all tile HLDs for all top row side tiles (60 inputs on each of 4 sides, including the two bottom rows).

IV. These three (3) lines are for use in selecting events for ACD tile calibration (they will need command adjustable pre-scaling to adjust rates):

- 7.) “OR” of all tile VETOs on each of the sides (4) sides (60 inputs on each of 4 sides, including the two bottom rows), each combined in an AND with its opposite producing a net of two (2) signals.
- 8.) “OR” of all tile VETOs on the top (25 inputs).

The first mentioned (1 above) is probably the least likely to be used at level1 and may be dropped. We may want to subdivide 1, 2, and 3 into subsets involving each side and the top. This would turn 3 into 15 signals and increase the total number of primitives from 24 to 36. But it would allow us to increase the flexibility to reject background depending on which tower was triggered and where the energy is deposited. In this case we might make better use of the segmentation of the lower rows of tiles.

Note that for PHA readout, the individual tiles to be read out on acceptance of a trigger will be those for which the signal exceeded the LLD. We can limit the number of PHA read to 4 (TBR) per event.

A special mode to read out pedestals should dump PHA outputs from all tiles.

A map of hit tiles will be made available for each event. The map is not currently part of the “trigger primitives” to be used at L1; the map is to be sent to the electronics for use in higher level triggers.

Conclusion: I recommend we attempt to accommodate 36 lines (one connector??) for trigger primitives. This will give us plenty of spares and when the L1 trigger, the rate capabilities of the electronics and the interface wiring are better defined we may be able to drop back to a number close to 24.