



GLAST

The Gamma Ray Large Area Space Telescope

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Gamma-ray Large Area Space Telescope (GLAST) Large Area Telescope (LAT) Anti-Coincidence Detector (ACD)

FREE (Front End & Event Electronics)



Thermal Performance Test

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1.0 Scope and Purpose of this Procedure

This document describes the instructions for the Thermal Testing of the FREE electronics assembly. It does not duplicate all the functions of component-level testing, but instead concentrates on board-level verification issues. This procedure provides the instructions necessary to functionally test the FREE assembly under thermal conditions.

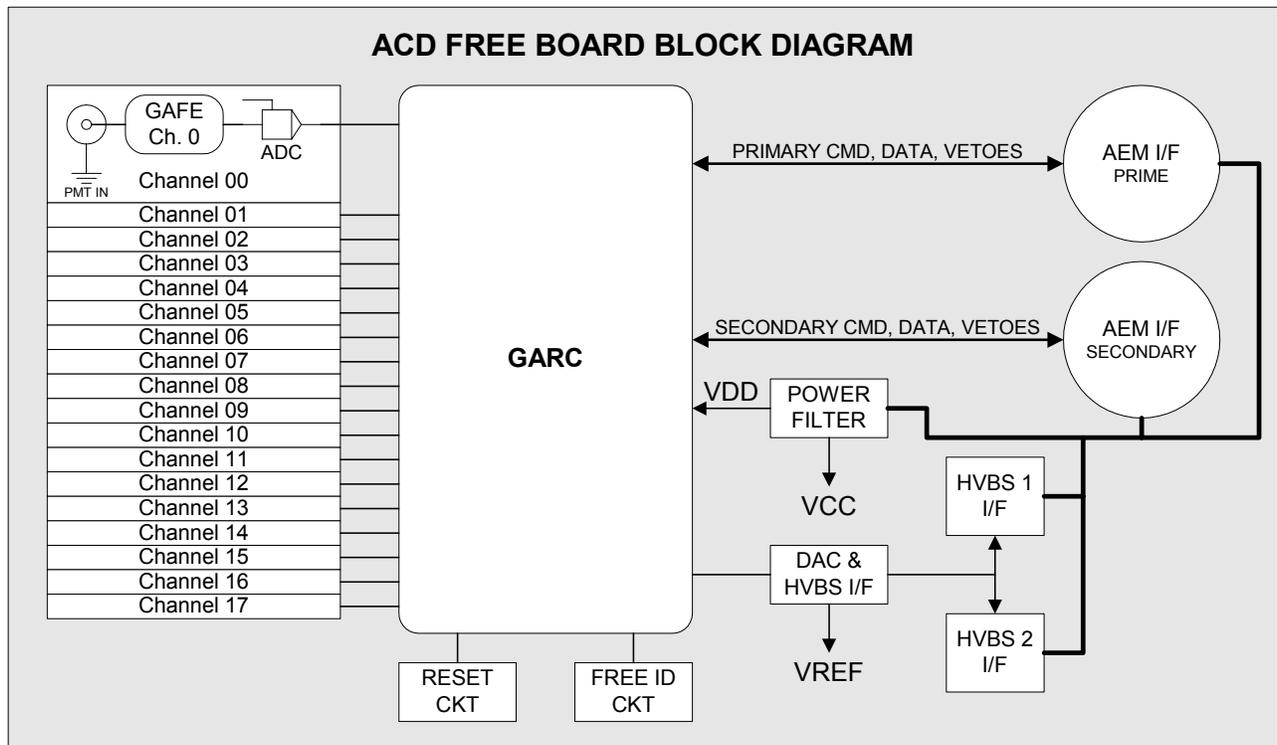
This test will be run at Room Temp., +60C and at -30C. The Power will be on during temperature transitions and the board will be allowed to soak at the test temperature for 30mins prior to starting the test.

The FREE assembly is designed to meet the electrical specifications of:

- (1) The ACD Level IV Electronics Requirements, LAT-SS-00352
- (2) The ACD-LAT Interface Control Document, LAT-SS-00-363

2.0 Description of the FREE Electronics Assembly

FREE is the acronym for the Gamma-Ray Large Area Space Telescope (GLAST) Anti-Coincidence Detector (ACD) Front End and Event Electronics processing board. The FREE provides the main electrical interface between the ACD and the LAT instrument electronics. The FREE circuitry provides command and data return functions for electronics boards associated with the ACD. There are 12 FREE boards in the flight system, with each FREE card supporting 18 phototube chains and 2 high voltage bias supplies (HVBS). The FREE circuitry utilizes a single +3.3V power supply and provides an interface to pass +28V power to the two HVBS. The FREE is a 10 layer flexible-rigid printed circuit board. It has 18 analog signal processing channels serviced by a single GARC readout controller. It also provides the interface to the HVBS and has two thermistors on board.



The design of the FREE circuitry was done utilizing Orcad for schematic capture, PSpice for simulation, and PADS for board layout. The current copy of the schematic package is posted in PDF format on the ACD website at: <http://lhea-glast.gsfc.nasa.gov/acd/electronics/#free>

3.0 Preconditions to and Preparations for Starting this Test

Prior to starting this test, a responsible Test Conductor shall be named. The Test Conductor is responsible for the safety of the hardware and the documentation of results, including anomalies, for the duration of the test. The Test Conductor, or a designated representative, shall be present for each testing sequence. All testing on flight hardware will require a signed Work Authorization Order. Each person working directly with the ACD flight hardware shall be NASA certified for electrostatic discharge control as per NASA-STD-8739.7. All measurement equipment used for verification tests on flight hardware shall have a valid calibration sticker. The Test Conductor shall have the authority to determine deviations from this procedure and shall redline this procedure as necessary. Mates and demates to flight connectors shall be recorded. Connectors shall not be mated nor demated unless the instrument electronics is powered off. Connector savers shall be utilized wherever practical to minimize flight connector mate/demates.

Notify QA 24 hours prior to the start of this test. QA will verify test equipment set up and calibration, review documentation and decide if their presence is required during the testing. Indicate on the test record whether QA was present for the testing.

All measurements and test results will be recorded in the "Test Results Record" Appendix 8. A copy of the entire this entire document is not required each time the test is performed. The appendix will serve as the official record each time this test is performed.

A dry nitrogen purge will be required for the thermal chamber during all phases of this test. The purge rate shall be no less than 2SCFH.

3.1 FREE Assembly Identification

Chamber Temperature: _____

The test conductor for this test is: _____

Date of Test: _____

The serial number of the FREE card assembly is: _____

The identification/Serial Number listed on the GARC ASIC is: _____

The identification/Serial Numbers listed on the GAFE ASICs are:

GAFE Channel	ASIC Serial Number
0	
1	
2	
3	
4	
5	
6	
7	
8	
9	
10	

11	
12	
13	
14	
15	
16	
17	

Note the performance of this test must be listed on the appropriate Work Authorization Order (WOA).

3.2 Test Equipment Utilized

Prior to starting this test, the Test Conductor shall record the test and measurement hardware used in the performance of this test. Note that all multimeters used in testing of the FREE circuit card assembly shall be of low current output design, such as the Fluke 70 series, HP3400 series or similar. High current output multimeters are not compatible with the FREE circuitry.

Instrument Type	Manufacturer & Model Number	NASA ID Number	Calibration Due Date
Power Supply for FREE & GSE +3.3V & +5.0V			
Multimeter 1			
Multimeter 2			
Oscilloscope			
Pulse Generator			
Tail Pulse Generator			
Charge Terminator Box			
Temperature Sensor			

3.3 Verification of the GSE Ground

Prior to the connection of FREE assembly hardware to other electronics, it shall be verified that all power supplies, signal generators, VME racks, and any other test and measurement equipment shall be connected to the same AC ground. The simplest way to do this is to connect all AC-powered equipment to the same power strip. In cases where this is not practical (e.g., possibly a thermal-vacuum test), greater care must be taken to ensure there are no floating grounds since this would represent a hazard to the FREE assembly.

4.0 Electrical Safe-to-Mate Verification

The intent of this section is to ensure that the AEM GSE is electrically safe to mate to the FREE assembly to be used for testing. Break Out Boxes (BOB) and a calibrated multimeter will be required for this test.

This section is to be performed prior to doing electrical testing on the FREE assembly. If this verification has been performed successfully, the Test Conductor may opt to omit this portion of the test if both the FREE assembly and the AEM interface have been checked.

1. Verify that connector savers have been installed on FREE connectors JP1, JS2, JHV1, and JHV2.
2. Verify that break out boxes (BOB) are available for these four connectors. These BOB should have been pin-for-pin checked for continuity and isolation prior to the start of this procedure.
3. The test conductor shall visually inspect each of the connector halves on the FREE assembly, BOB, harnessing, and AEM interface to ensure there are no bent pins, debris, or other physical damage that would impede safe connector mating.
4. All shorting pins should be removed from the BOBs.
5. Verify that the power supplies are OFF.
6. Mate the four BOBs to connectors JP1, JS2, JHV1 and JHV2 on the FREE assembly. Mate the other side of the BOBs to the AEM interface connectors.

4.1 Verification of Proper LVDS Terminations

The ACD interface requires proper termination of the LVDS drivers. The specification is $100\ \Omega \pm 5\%$. This test is performed with the ACD power off. A multimeter is used to measure the impedance across the following signal pairs on the GSE side of the BOB and the result is recorded

This test may be omitted at the discretion of the Test Conductor.

Measurement No.	Signal Pair	Pin 1	Pin 2	Expected Resistance	Verified
1	ACD_NVETO_16_A	JP1 - 17	JP1 - 18	$95\ \Omega < R < 105\ \Omega$	
2	ACD_NVETO_17_A	JP1 - 19	JP1 - 20	$95\ \Omega < R < 105\ \Omega$	
3	ACD_CNO_A	JP1 - 21	JP1 - 22	$95\ \Omega < R < 105\ \Omega$	
4	ACD_NVETO_15_A	JP1 - 40	JP1 - 41	$95\ \Omega < R < 105\ \Omega$	
5	ACD_NVETO_14_A	JP1 - 42	JP1 - 43	$95\ \Omega < R < 105\ \Omega$	
6	ACD_NVETO_13_A	JP1 - 44	JP1 - 45	$95\ \Omega < R < 105\ \Omega$	
7	ACD_NVETO_12_A	JP1 - 46	JP1 - 47	$95\ \Omega < R < 105\ \Omega$	
8	ACD_NVETO_11_A	JP1 - 48	JP1 - 49	$95\ \Omega < R < 105\ \Omega$	
9	ACD_NVETO_10_A	JP1 - 50	JP1 - 51	$95\ \Omega < R < 105\ \Omega$	
10	ACD_NVETO_09_A	JP1 - 52	JP1 - 53	$95\ \Omega < R < 105\ \Omega$	
11	ACD_NVETO_08_A	JP1 - 54	JP1 - 55	$95\ \Omega < R < 105\ \Omega$	
12	ACD_NVETO_07_A	JP1 - 56	JP1 - 57	$95\ \Omega < R < 105\ \Omega$	
13	ACD_NVETO_06_A	JP1 - 58	JP1 - 59	$95\ \Omega < R < 105\ \Omega$	
14	ACD_NVETO_05_A	JP1 - 60	JP1 - 61	$95\ \Omega < R < 105\ \Omega$	
15	ACD_NVETO_04_A	JP1 - 62	JP1 - 63	$95\ \Omega < R < 105\ \Omega$	
16	ACD_NVETO_03_A	JP1 - 64	JP1 - 65	$95\ \Omega < R < 105\ \Omega$	
17	ACD_NVETO_02_A	JP1 - 66	JP1 - 67	$95\ \Omega < R < 105\ \Omega$	
18	ACD_NVETO_01_A	JP1 - 68	JP1 - 69	$95\ \Omega < R < 105\ \Omega$	
19	ACD_NVETO_00_A	JP1 - 70	JP1 - 71	$95\ \Omega < R < 105\ \Omega$	
20	ACD_NSDATA_A	JP1 - 72	JP1 - 73	$95\ \Omega < R < 105\ \Omega$	
21	ACD_NRST_A	JP1 - 74	JP1 - 75	$R > 100\ \text{k}\Omega$	
22	ACD_NSCMD_A	JP1 - 76	JP1 - 77	$R > 100\ \text{k}\Omega$	
23	ACD_CLK_A	JP1 - 78	JP1 - 79	$R > 100\ \text{k}\Omega$	

24	ACD_NVETO_16_B	JS2 - 17	JS2 - 18	95 Ω < R < 105 Ω	
25	ACD_NVETO_17_B	JS2 - 19	JS2 - 20	95 Ω < R < 105 Ω	
26	ACD_CNO_B	JS2 - 21	JS2 - 22	95 Ω < R < 105 Ω	
27	ACD_NVETO_15_B	JS2 - 40	JS2 - 41	95 Ω < R < 105 Ω	
28	ACD_NVETO_14_B	JS2 - 42	JS2 - 43	95 Ω < R < 105 Ω	
29	ACD_NVETO_13_B	JS2 - 44	JS2 - 45	95 Ω < R < 105 Ω	
30	ACD_NVETO_12_B	JS2 - 46	JS2 - 47	95 Ω < R < 105 Ω	
31	ACD_NVETO_11_B	JS2 - 48	JS2 - 49	95 Ω < R < 105 Ω	
32	ACD_NVETO_10_B	JS2 - 50	JS2 - 51	95 Ω < R < 105 Ω	
33	ACD_NVETO_09_B	JS2 - 52	JS2 - 53	95 Ω < R < 105 Ω	
34	ACD_NVETO_08_B	JS2 - 54	JS2 - 55	95 Ω < R < 105 Ω	
35	ACD_NVETO_07_B	JS2 - 56	JS2 - 57	95 Ω < R < 105 Ω	
36	ACD_NVETO_06_B	JS2 - 58	JS2 - 59	95 Ω < R < 105 Ω	
37	ACD_NVETO_05_B	JS2 - 60	JS2 - 61	95 Ω < R < 105 Ω	
38	ACD_NVETO_04_B	JS2 - 62	JS2 - 63	95 Ω < R < 105 Ω	
39	ACD_NVETO_03_B	JS2 - 64	JS2 - 65	95 Ω < R < 105 Ω	
40	ACD_NVETO_02_B	JS2 - 66	JS2 - 67	95 Ω < R < 105 Ω	
41	ACD_NVETO_01_B	JS2 - 68	JS2 - 69	95 Ω < R < 105 Ω	
42	ACD_NVETO_00_B	JS2 - 70	JS2 - 71	95 Ω < R < 105 Ω	
43	ACD_NSDATA_B	JS2 - 72	JS2 - 73	95 Ω < R < 105 Ω	
44	ACD_NRST_B	JS2 - 74	JS2 - 75	R > 100 k Ω	
45	ACD_NSCMD_B	JS2 - 76	JS2 - 77	R > 100 k Ω	
46	ACD_CLK_B	JS2 - 78	JS2 - 79	R > 100 k Ω	

4.2 Stray Voltage Test at the AEM Interface

With the shorting plugs removed from the break out boxes, turn the ACD power on and perform the following voltage measurements on the AEM interface side of the break out box. The (-) input to the voltmeter may be referenced to pin 30, the +3.3V return.

This test may be omitted at the discretion of the Test Conductor.

Meas. No.	AEM Interface Pin	Signal Name	Expected Voltage	Measured Voltage
1	JP1 - 1	ACD_VDD_0A	+3.3V	
2	JP1 - 3	ACD_VDD_1A	+3.3V	
3	JP1 - 4	ACD_VDD_2A	+3.3V	
4	JP1 - 5	ACD_28V_0A	+28V	
5	JP1 - 7	ACD_28V_1A	+28V	
6	JP1 - 17	ACD_NVETO_16AP	0 < V < 3.3	
7	JP1 - 18	ACD_NVETO_16AM	0 < V < 3.3	
8	JP1 - 19	ACD_NVETO_17AP	0 < V < 3.3	
9	JP1 - 20	ACD_NVETO_17AM	0 < V < 3.3	
10	JP1 - 21	ACD_NCNO_AP	0 < V < 3.3	
11	JP1 - 22	ACD_NCNO_AM	0 < V < 3.3	
12	JP1 - 23	ACD_HV_AP	0 < V < 3.3	
13	JP1 - 24	ACD_HV_AM	0 < V < 3.3	
14	JP1 - 25	ACD_TEMP_AP	0	
15	JP1 - 26	ACD_TEMP_AM	0	
17	JP1 - 31	ACD_GND_1A	0	
18	JP1 - 32	ACD_GND_2A	0	

19	JP1 - 33	ACD_28V_RTN_0A	0	
20	JP1 - 34	ACD_28V_RTN_1A	0	
21	JP1 - 40	ACD_NVETO_15AM	V < 200mV	
22	JP1 - 41	ACD_NVETO_15AP	V < 200mV	
23	JP1 - 42	ACD_NVETO_14AM	V < 200mV	
24	JP1 - 43	ACD_NVETO_14AP	V < 200mV	
25	JP1 - 44	ACD_NVETO_13AM	V < 200mV	
26	JP1 - 45	ACD_NVETO_13AP	V < 200mV	
27	JP1 - 46	ACD_NVETO_12AM	V < 200mV	
28	JP1 - 47	ACD_NVETO_12AP	V < 200mV	
29	JP1 - 48	ACD_NVETO_11AM	V < 200mV	
31	JP1 - 50	ACD_NVETO_10AM	V < 200mV	
32	JP1 - 51	ACD_NVETO_10AP	V < 200mV	
33	JP1 - 52	ACD_NVETO_09AM	V < 200mV	
34	JP1 - 53	ACD_NVETO_09AP	V < 200mV	
35	JP1 - 54	ACD_NVETO_08AM	V < 200mV	
36	JP1 - 55	ACD_NVETO_08AP	V < 200mV	
37	JP1 - 56	ACD_NVETO_07AM	V < 200mV	
38	JP1 - 57	ACD_NVETO_07AP	V < 200mV	
39	JP1 - 58	ACD_NVETO_06AM	V < 200mV	
40	JP1 - 59	ACD_NVETO_06AP	V < 200mV	
41	JP1 - 60	ACD_NVETO_05AM	V < 200mV	
42	JP1 - 61	ACD_NVETO_05AP	V < 200mV	
43	JP1 - 62	ACD_NVETO_04AM	V < 200mV	
44	JP1 - 63	ACD_NVETO_04AP	V < 200mV	
45	JP1 - 64	ACD_NVETO_03AM	V < 200mV	
46	JP1 - 65	ACD_NVETO_03AP	V < 200mV	
47	JP1 - 66	ACD_NVETO_02AM	V < 200mV	
48	JP1 - 67	ACD_NVETO_02AP	V < 200mV	
49	JP1 - 68	ACD_NVETO_01AM	V < 200mV	
50	JP1 - 69	ACD_NVETO_01AP	V < 200mV	
51	JP1 - 70	ACD_NVETO_00AM	V < 200mV	
52	JP1 - 71	ACD_NVETO_00AP	V < 200mV	
53	JP1 - 72	ACD_NSDATA_AM	V < 200mV	
54	JP1 - 73	ACD_NSDATA_AP	V < 200mV	
55	JP1 - 74	ACD_NRST_AM	V < 200mV	
56	JP1 - 75	ACD_NRST_AP	V > 2.3V	
57	JP1 - 76	ACD_NSCMD_AM	V < 200mV	
58	JP1 - 77	ACD_NSCMD_AP	V > 2.3V	
59	JP1 - 78	ACD_CLK_AM	1.1V < V < 1.5V	
60	JP1 - 79	ACD_CLK_AP	1.1V < V < 1.5V	
61	JS2 - 1	ACD_VDD_0B	+3.3V	
62	JS2 - 3	ACD_VDD_1B	+3.3V	
63	JS2 - 4	ACD_VDD_2B	+3.3V	
64	JS2 - 5	ACD_28V_0B	+28V	
65	JS2 - 7	ACD_28V_1B	+28V	
66	JS2 - 17	ACD_NVETO_16BP	V < 200mV	
67	JS2 - 18	ACD_NVETO_16BM	V < 200mV	
68	JS2 - 19	ACD_NVETO_17BP	V < 200mV	
69	JS2 - 20	ACD_NVETO_17BM	V < 200mV	
70	JS2 - 21	ACD_NCNO_BP	V < 200mV	

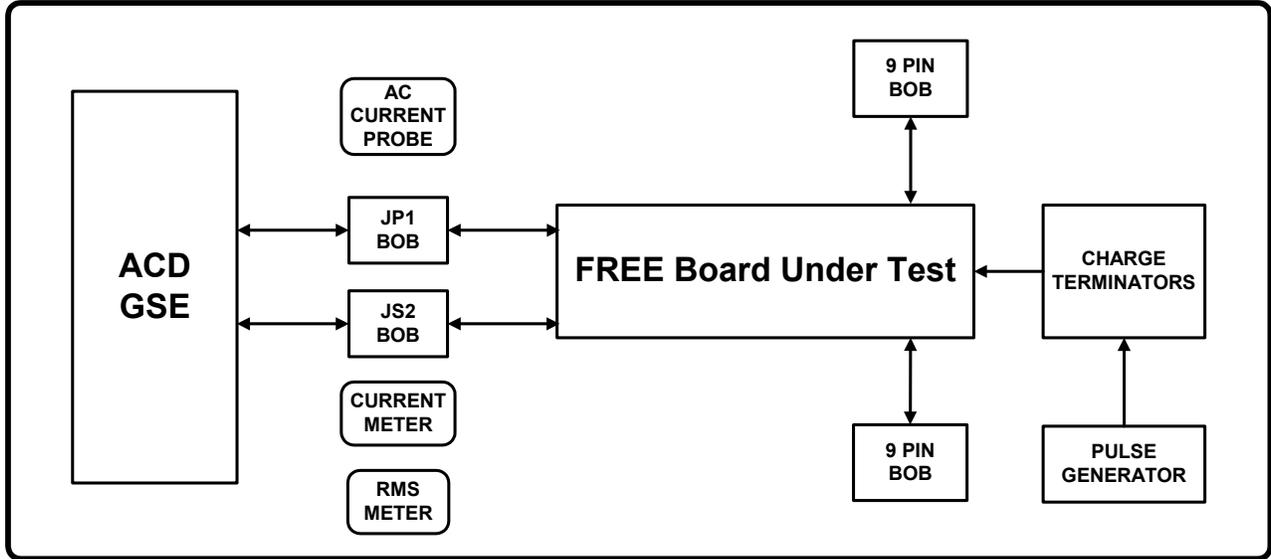
71	JS2 - 22	ACD_NCNO_BM	V < 200mV	
72	JS2 - 23	ACD_HV_BP	V < 200mV	
73	JS2 - 24	ACD_HV_BM	V < 200mV	
74	JS2 - 25	ACD_TEMP_BP	0	
75	JS2 - 26	ACD_TEMP_BM	0	
76	JS2 - 30	ACD_GND_0B	0	
77	JS2 - 31	ACD_GND_1B	0	
78	JS2 - 32	ACD_GND_2B	0	
79	JS2 - 33	ACD_28V_RTN_0B	0	
80	JS2 - 34	ACD_28V_RTN_1B	0	
81	JS2 - 40	ACD_NVETO_15BM	V < 200mV	
82	JS2 - 41	ACD_NVETO_15BP	V < 200mV	
83	JS2 - 42	ACD_NVETO_14BM	V < 200mV	
84	JS2 - 43	ACD_NVETO_14BP	V < 200mV	
85	JS2 - 44	ACD_NVETO_13BM	V < 200mV	
86	JS2 - 45	ACD_NVETO_13BP	V < 200mV	
87	JS2 - 46	ACD_NVETO_12BM	V < 200mV	
88	JS2 - 47	ACD_NVETO_12BP	V < 200mV	
89	JS2 - 48	ACD_NVETO_11BM	V < 200mV	
90	JS2 - 49	ACD_NVETO_11BP	V < 200mV	
91	JS2 - 50	ACD_NVETO_10BM	V < 200mV	
92	JS2 - 51	ACD_NVETO_10BP	V < 200mV	
93	JS2 - 52	ACD_NVETO_09BM	V < 200mV	
94	JS2 - 53	ACD_NVETO_09BP	V < 200mV	
95	JS2 - 54	ACD_NVETO_08BM	V < 200mV	
96	JS2 - 55	ACD_NVETO_08BP	V < 200mV	
97	JS2 - 56	ACD_NVETO_07BM	V < 200mV	
98	JS2 - 57	ACD_NVETO_07BP	V < 200mV	
99	JS2 - 58	ACD_NVETO_06BM	V < 200mV	
100	JS2 - 59	ACD_NVETO_06BP	V < 200mV	
101	JS2 - 60	ACD_NVETO_05BM	V < 200mV	
102	JS2 - 61	ACD_NVETO_05BP	V < 200mV	
103	JS2 - 62	ACD_NVETO_04BM	V < 200mV	
104	JS2 - 63	ACD_NVETO_04BP	V < 200mV	
105	JS2 - 64	ACD_NVETO_03BM	V < 200mV	
106	JS2 - 65	ACD_NVETO_03BP	V < 200mV	
107	JS2 - 66	ACD_NVETO_02BM	V < 200mV	
108	JS2 - 67	ACD_NVETO_02BP	V < 200mV	
109	JS2 - 68	ACD_NVETO_01BM	V < 200mV	
110	JS2 - 69	ACD_NVETO_01BP	V < 200mV	
111	JS2 - 70	ACD_NVETO_00BM	V < 200mV	
112	JS2 - 71	ACD_NVETO_00BP	V < 200mV	
113	JS2 - 72	ACD_NSDATA_BM	V < 200mV	
114	JS2 - 73	ACD_NSDATA_BP	V < 200mV	
115	JS2 - 74	ACD_NRST_BM	V < 200mV	
116	JS2 - 75	ACD_NRST_BP	V > 2.3V	
117	JS2 - 76	ACD_NSCMD_BM	V < 200mV	
118	JS2 - 77	ACD_NSCMD_BP	V > 2.3V	
119	JS2 - 78	ACD_CLK_BM	1.1V < V < 1.5V	
120	JS2 - 79	ACD_CLK_BP	1.1V < V < 1.5V	

4.3 Removal of Breakout Boxes

Remove the break out boxes on connectors JP1, JS2. The pin connections for the two 79 pin circular connectors JP1 and JS2 are listed in Appendix 6. The pin connections for the two 9 pin MDM connectors to the High Voltage Bias Supplies are listed in Appendix 5.

5.0 Testing the FREE Electronics via Command-Response Protocol

The GARC logic is based on a command-response protocol and requires an AEM or AEM simulator to access the logic functions. For each of the following commands, the proper GARC and/or GAFE response may be tested. The test setup required is detailed in the diagram below.



This section of the test will verify the general aliveness of the powered-on FREE circuit assembly. This test will be run at Room Temp., +60C and at -30C. The Power will be on during temperature transitions and the board will be allowed to soak at the test temperature for 30mins prior to starting the test.

5.1 GARC and GAFE Registers Initial Reset Test

This section will verify that GARC registers have been properly initialized during a reset command. The following test sequence of commands will perform this verification. This test will also verify that the GARC to AEM command and data return link is functional. At the successful conclusion of this section, please document this fact by making an entry in the copy of the Comprehensive Performance Test Record associated with this procedure.

Record the following Temperatures

- Chamber Temperature - _____
- Board Temperature - _____
- GARC Temperature - _____

Turn on the power supplies then –

1. Record the +3.3V Current - _____
2. Verify the external GARC Power On Reset pulse. Send the Look at Me command then the Read All Values command.
3. Send the Veto_Delay_Rd command. The data field in the return data stream should be 5.

4. Send the HVBS_Level_Rd command. The data field in the return data stream should be 0.
5. Send the SAA_Level_Rd command. The data field in the return data stream should be 0.
6. Send the Hold_Delay_Rd command. The data field in the return data stream should be 28.
7. Send the Veto_Width_Rd command. The data field in the return data stream should be 2.
8. Send the HitMap_Width_Rd command. The data field in the return data stream should be 7.
9. Send the HitMap_Deadtime_Rd command. The data field in the return data stream should be 3.
10. Send the HitMap_Delay_Rd command. The data field in the return data stream should be 16.
11. Send the PHA_En0_Rd command. The data field in the return data stream should be 65535.
12. Send the PHA_En1_Rd command. The data field in the return data stream should be 3.
13. Send the Veto_En0_Rd command. The data field in the return data stream should be 65535.
14. Send the Veto_En1_Rd command. The data field in the return data stream should be 3.
15. Send the Max_PHA_Rd command. The data field in the return data stream should be 4.
16. Send the GARC_Mode_Rd command. The data field in the return data stream should be 768.
17. Send the GARC_Status command. The data field in the return data stream should be 24.
18. Send the GARC_Cmd_Reg command. The data field in the return data stream should be 0.
19. Send the GARC_Cmd_Rejects command. The data field in the return data stream should be 0.
20. Send the GARC_Version command. The data field in the return data stream should be 3 for GARC V3 ASICs.
21. Send the PHA_Thresh00_Rd command. The data field in the return data stream should be 1114.
22. Send the PHA_Thresh01_Rd command. The data field in the return data stream should be 1114.
23. Send the PHA_Thresh02_Rd command. The data field in the return data stream should be 1114.
24. Send the PHA_Thresh03_Rd command. The data field in the return data stream should be 1114.
25. Send the PHA_Thresh04_Rd command. The data field in the return data stream should be 1114.
26. Send the PHA_Thresh05_Rd command. The data field in the return data stream should be 1114.
27. Send the PHA_Thresh06_Rd command. The data field in the return data stream should be 1114.
28. Send the PHA_Thresh07_Rd command. The data field in the return data stream should be 1114.
29. Send the PHA_Thresh08_Rd command. The data field in the return data stream should be 1114.
30. Send the PHA_Thresh09_Rd command. The data field in the return data stream should be 1114.
31. Send the PHA_Thresh10_Rd command. The data field in the return data stream should be 1114.
32. Send the PHA_Thresh11_Rd command. The data field in the return data stream should be 1114.
33. Send the PHA_Thresh12_Rd command. The data field in the return data stream should be 1114.
34. Send the PHA_Thresh13_Rd command. The data field in the return data stream should be 1114.
35. Send the PHA_Thresh14_Rd command. The data field in the return data stream should be 1114.
36. Send the PHA_Thresh15_Rd command. The data field in the return data stream should be 1114.
37. Send the PHA_Thresh16_Rd command. The data field in the return data stream should be 1114.
38. Send the PHA_Thresh17_Rd command. The data field in the return data stream should be 1114.

39. Send the ADC_TACQ_Rd command. The data field in the return data stream should be 0.
40. Send the Trigger_ZS command (this captures the FREE board ID). FREE board ID should be as recorded on the WOA.

Record FREE board ID - _____

41. Send the GARC_Reset command (Do Reset Pulse from the Labview Program).
42. Check the FREE board ID. It should be 255, indicating a Reset had occurred.

Record FREE board ID - _____

43. Verify the status of the GARC registers as shown in steps 2 – 39 above.

If all steps above have verified correctly, the GARC reset function has been verified.

5.2 GARC/GAFE Register Read/Write Tests

This section tests the proper functioning of each bit of the commandable registers in the GARC. The intent is to toggle each bit in a variety of patterns to ensure that all bits are addressable and that there is no stuck-at-fault condition. This can be accomplished using the LabView GSE software by running the Register Test 3 times with all GAFE registers enabled.

5.3 FREE Power Measurement at the Nominal Power Supply Voltage

Verify that the GARC power supply is set to +3.30V. After initial power up, measure the +3.30V power supply current to the GARC in the following modes. Record these values in the table below.

1. Send the GARC_Mode_Wr command with a data argument of 768. Send the GARC_Mode_Rd command to verify. Both the primary and secondary LVDS VETO drivers should be enabled. Record the GARC current in the table below.
2. Send the GARC_Mode_Wr command with a data argument of 256. Send the GARC_Mode_Rd command to verify. Only the primary LVDS VETO drivers should now be enabled. Record the GARC current in the table below.
3. Send the GARC_Mode_Wr command with a data argument of 512. Send the GARC_Mode_Rd command to verify. Only the secondary LVDS VETO drivers should now be enabled. Record the GARC current in the table below.
4. Send the GARC_Mode_Wr command with a data argument of 0. Send the GARC_Mode_Rd command to verify. None of the LVDS VETO drivers should now be enabled. Record the GARC current in the table below.

GARC Mode	GARC_Mode_Wr Data Argument	+3.3V Current Measured (mA)	+3.3V Current Expected (mA)
LVDS "A" Drivers Enabled LVDS "B" Drivers Enabled	768		200 ± 10mA
LVDS "A" Drivers Enabled LVDS "B" Drivers Disabled	256		150 ± 10mA
LVDS "A" Drivers Disabled LVDS "B" Drivers Enabled	512		150 ± 10mA
LVDS "A" Drivers Disabled LVDS "B" Drivers Disabled	0		95 ± 10mA

5.4 FREE Power Measurement at the Minimum Power Supply Voltage

Verify that the GARC power supply is set to +3.0V. After initial power up, measure the +3.0V power supply current to the GARC in the following modes. Record these values in the table below.

1. Send the GARC_Mode_Wr command with a data argument of 768. Send the GARC_Mode_Rd command to verify. Both the primary and secondary LVDS VETO drivers should be enabled. Record the GARC current in the table below.
2. Send the GARC_Mode_Wr command with a data argument of 256. Send the GARC_Mode_Rd command to verify. Only the primary LVDS VETO drivers should now be enabled. Record the GARC current in the table below.
3. Send the GARC_Mode_Wr command with a data argument of 512. Send the GARC_Mode_Rd command to verify. Only the secondary LVDS VETO drivers should now be enabled. Record the GARC current in the table below.
4. Send the GARC_Mode_Wr command with a data argument of 0. Send the GARC_Mode_Rd command to verify. None of the LVDS VETO drivers should now be enabled. Record the GARC current in the table below.

GARC Mode	GARC_Mode_Wr Data Argument	+3.0V Current Measured (mA)	+3.0V Current Expected (mA)
LVDS "A" Drivers Enabled LVDS "B" Drivers Enabled	768		170 ± 10mA
LVDS "A" Drivers Enabled LVDS "B" Drivers Disabled	256		125 ± 10mA
LVDS "A" Drivers Disabled LVDS "B" Drivers Enabled	512		125 ± 10mA
LVDS "A" Drivers Disabled LVDS "B" Drivers Disabled	0		75 ± 10mA

5.5 FREE Power Measurement at the Maximum Power Supply Voltage

Verify that the GARC power supply is set to +3.6V. After initial power up, measure the +3.6V power supply current to the GARC in the following modes. Record these values in the table below.

1. Send the GARC_Mode_Wr command with a data argument of 768. Send the GARC_Mode_Rd command to verify. Both the primary and secondary LVDS VETO drivers should be enabled. Record the GARC current in the table below.
2. Send the GARC_Mode_Wr command with a data argument of 256. Send the GARC_Mode_Rd command to verify. Only the primary LVDS VETO drivers should now be enabled. Record the GARC current in the table below.
3. Send the GARC_Mode_Wr command with a data argument of 512. Send the GARC_Mode_Rd command to verify. Only the secondary LVDS VETO drivers should now be enabled. Record the GARC current in the table below.
4. Send the GARC_Mode_Wr command with a data argument of 0. Send the GARC_Mode_Rd command to verify. None of the LVDS VETO drivers should now be enabled. Record the GARC current in the table below.

GARC Mode	GARC_Mode_Wr Data Argument	+3.6V Current Measured (mA)	+3.6V Current Expected (mA)
LVDS "A" Drivers Enabled LVDS "B" Drivers Enabled	768		230 ± 10mA
LVDS "A" Drivers Enabled LVDS "B" Drivers Disabled	256		175 ± 10mA
LVDS "A" Drivers Disabled LVDS "B" Drivers Enabled	512		175 ± 10mA
LVDS "A" Drivers Disabled LVDS "B" Drivers Disabled	0		115 ± 10mA

5. Reset the GARC power supply to +3.3V.
6. Send the GARC_Reset command to return the GARC to the initial power-on configuration.

5.6 Test of the Look-At-Me Circuitry

This section tests the proper functioning of the GARC Look-At-Me circuitry. The GARC has the capability to receive commands from either the primary side or secondary side. The selection of which set of receivers to listen to is controlled by the Look-At-Me circuitry. This circuitry toggles the status of the receiving side based upon receipt of a special command pattern (e.g., **34'h24153D721**). This the equivalent of sending a GARC configuration command to addr 1, function 4, with a data pattern of 60304.

Another way to look at the bit pattern (in a format like the ICD would present it) would be:

- 1001 == configuration command
- 0 == GARC
- 00001 == address 1
- 0 == write
- 1 == a command with data
- 0100 == function 4
- 1 == command parity
- 16'h == EB90 == data field (60304)
- 0 == data parity

This test may be automated using the LabView GSE via the GARC Look At Me Test.txt script.

Turn on the system and send a Look-at-me command. Send the GARC_Status command. The data field in the return data stream should be decimal 24. Bit 0 (LSB) of the Status register represents the Look-At-Me status (0 = A, 1 = B).. Set the GSE to the Secondary side, Send the GARC_Status command. Observe that there is no response from the GARC.

Send the Look_At_Me command to the GARC from the secondary side interface. Send the GARC_Status command. The data field in the return data should be decimal 25 (with the LSB = 1, indicating the Look-At-Me status is B side). Set the GSE for the Primary side and send the GARC_Status command. Observe that there is no response from the GARC. Send the Look_At_Me command to the GARC from the primary side interface. Send the GARC_Status command. The data field in the return data should be decimal 24 (with the LSB = 0, indicating the Look-At-Me status is A side).

This concludes the test of the GARC Look-At-Me circuitry. At the successful conclusion of this section, please document this fact by making an entry in the copy of the Comprehensive Performance Test Record associated with this procedure.

5.7 Test of the HVBS DAC Commands, DAC Buffer, and Differential Drivers

To verify the operation of the HVBS DAC and Differential Driver make the following measurements while sending the HVBS_Level_Wr command and Use_HV_Nominal_Wr command to change the DAC setting as shown to verify the linearity of the circuit.

This test may be automated using the LabView GSE via the GARC HVBS DAC Level Test.txt script. Gnd is at the Lepracon connector shield.

Meas. No.	DAC SETTING	JHV1-4 to JHV1-9 (HV-DAC)
1	0	
2	200	
3	400	
4	600	
5	800	
6	1000	
7	1200	
8	1400	
9	1600	
10	1800	
11	2000	
12	2200	
13	2400	
14	2600	
15	2800	
16	3000	
17	3200	
18	3400	
19	3600	
20	3800	
21	4000	
22	4095	

5.8 Test of the HVBS Triple Modular Redundancy Circuitry

This section tests the proper functioning of the GARC HVBS enable circuitry. Each pattern in the TMR logic will be tested to verify proper recovery from a single event upset. A truth table for proper TMR circuitry function is detailed below.

To verify the Enable command, connect a volt meter to JHV1-5 (HV_Enable_1) and JHV2-5 (HV_Enable_2) of the FREE board. Exact voltages for command on and off will be measured at the end of this section. For nominal power supply voltages, the nominal “ON” voltage is approximately 3.2V and “OFF” is approximately 0.015V. The ground reference shall be at the power supply.

This test may be automated using the LabView GSE via the GARC HV Enable Test.txt script. Gnd is at the Lepracon connector shield.

Enable Bit A	Enable Bit B	Enable Bit C	HV Enable Output
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

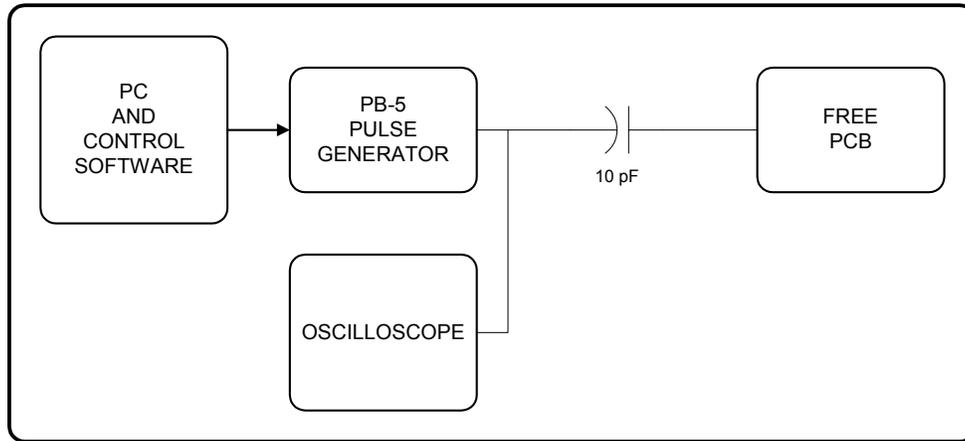
1. Send the GARC_Mode_Wr command with a data argument of 768 and verify the data with the GARC_Mode_Rd command.
2. Send the GARC_Status command. The data field in the return data stream should show that bits 1 and 2 are 0, indicating that HVBS 1 and 2, respectively, are disabled. The data field value should be 24. Verify that JHV1-5 (HV_Enable_1) and JHV2-5 (HV_Enable_2) are at 0V.
3. Send the GARC_Mode_Wr command with decimal argument 770 and verify the data with the GARC_Mode_Rd command. Send the GARC_Status command and verify that HVBS 1 is disabled and HVBS 2 is disabled. The data field value should be 24. Verify that JHV1-5 (HV_Enable_1) and JHV2-5 (HV_Enable_2) are at 0V.
4. Send the GARC_Mode_Wr command with decimal argument 772 and verify the data with the GARC_Mode_Rd command. Send the GARC_Status command and verify that HVBS 1 is disabled and HVBS 2 is disabled. The data field value should be 24. Verify that JHV1-5 (HV_Enable_1) and JHV2-5 (HV_Enable_2) are at 0V.
5. Send the GARC_Mode_Wr command with decimal argument 774 and verify the data with the GARC_Mode_Rd command. Send the GARC_Status command and verify that HVBS 1 is enabled and HVBS 2 is disabled. The data field value should be 26. Verify that JHV1-5 (HV_Enable_1) is at 3.3V and JHV2-5 (HV_Enable_2) is at 0V.
6. Send the GARC_Mode_Wr command with decimal argument 776 and verify the data with the GARC_Mode_Rd command. Send the GARC_Status command and verify that HVBS 1 is disabled and HVBS 2 is disabled. The data field value should be 24. Verify that JHV1-5 (HV_Enable_1) and JHV2-5 (HV_Enable_2) is at 0V.
7. Send the GARC_Mode_Wr command with decimal argument 778 and verify the data with the GARC_Mode_Rd command. Send the GARC_Status command and verify that HVBS 1 is enabled and HVBS 2 is disabled. The data field value should be 26. Verify that JHV1-5 (HV_Enable_1) and JHV2-5 (HV_Enable_2) is at 0V.
8. Send the GARC_Mode_Wr command with decimal argument 780 and verify the data with the GARC_Mode_Rd command. Send the GARC_Status command and verify that HVBS 1 is enabled and HVBS 2 is disabled. The data field value should be 26. Verify that JHV1-5 (HV_Enable_1) is at 3.3V and JHV2-5 (HV_Enable_2) is at 0V.
9. Send the GARC_Mode_Wr command with decimal argument 782 and verify the data with the GARC_Mode_Rd command. Send the GARC_Status command and verify that HVBS 1 is enabled and HVBS 2 is disabled. The data field value should be 26. Verify that JHV1-5 (HV_Enable_1) is at 3.3V and JHV2-5 (HV_Enable_2) is at 0V.

10. Send the GARC_Mode_Wr command with decimal argument 784 and verify the data with the GARC_Mode_Rd command. Send the GARC_Status command and verify that HVBS 1 is disabled and HVBS 2 is disabled. The data field value should be 24. Verify that JHV1-5 (HV_Enable_1) and JHV2-5 (HV_Enable_2) is at 0V.
11. Send the GARC_Mode_Wr command with decimal argument 800 and verify the data with the GARC_Mode_Rd command. Send the GARC_Status command and verify that HVBS 1 is disabled and HVBS 2 is disabled. The data field value should be 24. Verify that JHV1-5 (HV_Enable_1) and JHV2-5 (HV_Enable_2) is at 0V.
12. Send the GARC_Mode_Wr command with decimal argument 816 and verify the data with the GARC_Mode_Rd command. Send the GARC_Status command and verify that HVBS 1 is disabled and HVBS 2 is enabled. The data field value should be 28. Verify that JHV1-5 (HV_Enable_1) is at 0V and JHV2-5 (HV_Enable_2) is at 3.3V.
13. Send the GARC_Mode_Wr command with decimal argument 832 and verify the data with the GARC_Mode_Rd command. Send the GARC_Status command and verify that HVBS 1 is disabled and HVBS 2 is disabled. The data field value should be 24. Verify that JHV1-5 (HV_Enable_1) and JHV2-5 (HV_Enable_2) is at 0V.
14. Send the GARC_Mode_Wr command with decimal argument 848 and verify the data with the GARC_Mode_Rd command. Send the GARC_Status command and verify that HVBS 1 is disabled and HVBS 2 is enabled. The data field value should be 28. Verify that JHV1-5 (HV_Enable_1) is at 0V and JHV2-5 (HV_Enable_2) is at 3.3V.
15. Send the GARC_Mode_Wr command with decimal argument 864 and verify the data with the GARC_Mode_Rd command. Send the GARC_Status command and verify that HVBS 1 is disabled and HVBS 2 is enabled. The data field value should be 28. Verify that JHV1-5 (HV_Enable_1) is at 0V and JHV2-5 (HV_Enable_2) is at 3.3V.
16. Send the GARC_Mode_Wr command with decimal argument 880 and verify the data with the GARC_Mode_Rd command. Send the GARC_Status command and verify that HVBS 1 is disabled and HVBS 2 is enabled. The data field value should be 28. Verify that JHV1-5 (HV_Enable_1) is at 0V and JHV2-5 (HV_Enable_2) is at 3.3V.
17. Send the GARC_Mode_Wr command with decimal argument 782 and verify the data with the GARC_Mode_Rd command. Measure the voltage at the two HV_ENABLE pins:
 - a. HV_ENABLE_1 voltage JHV1-5: _____ (expected ~ 3.2V)
 - b. HV_ENABLE_2 voltage JHV2-5: _____ (expected ~ 3.2V)
18. Send the GARC_Mode_Wr command with decimal argument 768 and verify the data with the GARC_Mode_Rd command. Measure the voltage at the two HV_ENABLE pins:
 - a. HV_ENABLE_1 voltage JHV1-5: _____ (expected ~ 0.015V)
 - b. HV_ENABLE_2 voltage JHV2-5: _____ (expected ~ 0.015V)
19. Send the GARC_Reset command. Verify that JHV1-5 (HV_Enable_1) and JHV2-5 (HV_Enable_2) is at 0V.

5.9 Characterization of each of the 18 GAFE chips

This test will verify the operation for each GAFE ASIC on the FREE printed circuit card. Included in this test will be the ADC conversion values as measured at the GARC. The low-energy threshold will be characterized during this test. The HLD enable/disable function will be tested.

A 10 pF charge terminator will be used for the each FREE board channel in the following setup.



In this case, the charge input to the FREE card is $Q = C \cdot V$, so 0.64 pC is approximately 64 mV on the scope. Run the automatic characterization script to test the following

- 1) Register test
- 2) Bias DAC Test (LE)
- 3) Bias DAC Test (HE)
- 4) Hold Delay
- 5) INL Test (LE)
- 6) INL Test (HE)
- 7) Crossover point (LE/HE)
- 8) Hitmap Delay Test
- 9) Veto DAC Test
- 10) Vernier DAC Test
- 11) HLD DAC Test
- 12) TCI (LE)
- 13) TCI (HE)

All printouts are to be attached to the Test Results Record.

Data File Name - _____

5.10 GAFE Channel Baseline PHA Test

This test may be skipped at the discretion of the Test Conductor.

The function of this portion of the test is to record the Baseline PHA values of the individual GAFE channels. For this test, no signal will be connected to any of the GAFE channel inputs, the AEM simulator will be configured to send event triggers. In the absence of an input pulse, the ADC zero energy baseline will be analyzed and recorded in the table below.

GAFE Channel	ADC Conversion Baseline (channel number)
0	
1	
2	
3	
4	
5	
6	
7	
8	
9	
10	
11	
12	
13	
14	
15	
16	
17	

5.11 Multiple System Clock Speed Test at +3.0V and +3.6V

The function of this test is to verify operation of the GARC circuitry over the range of allowable clock frequencies and Power Supply Rail limits. The majority of this test has been performed at the nominal 20 MHz clock and has therefore verified the nominal frequency. This portion of the test will verify operation at the low and high limit frequencies and at min and max rail voltages. This will be verified by performing the register test and checking the operation of the DAC interface circuitry. This may be done via automated script.

- 1) Set the Power Supply to +3.0V
 +3.0V current - _____
- 2) Set the clock frequency to the 22 MHz high limit.
- 3) Run the register test from section 6
- 4) Run the test of the DAC interface circuitry, section 5.7
- 5) Set the Power Supply to +3.6V
 +3.6V current - _____
- 6) Run the register test from section 6
- 7) Run the test of the DAC interface circuitry, section 5.7
- 8) Set the clock frequency to the 14 MHz low limit leave the power supply set to +3.6V.

- 9) Run the register test from section 6
- 10) Run the test of the DAC interface circuitry, section 5.7
- 11) Set the Power Supply to +3.0V
- 12) Run the register test from section 6
- 13) Run the test of the DAC interface circuitry, section 5.7

Reset the clock frequency to the 20 MHz nominal.

5.12 Power Supply Rail Tests – 3.0V to 3.6V

Power supply rail voltage testing has been performed on both the GARC and GAFE ASICs prior to integration to the FREE card assembly. This test will verify the operation of the card at the upper and lower voltage limits of +3.60V and +3.00V, respectively. This test will repeat sections performed previously in this test, comparing the results.

- 1) Verify that the power supply is set to +3.0V.
- 2) Run the GAFE characterization test, section 5.9.

Record the File name - _____

- 3) Set the power supply to +3.6V.
- 4) Run the GAFE characterization test, section 5.9.

Record the File name - _____

6.0 Change Chamber Temperature

Change the chamber to the next temperature and repeat Section 5.

Appendix 1: GARC Documentation

A more complete set of documentation (such as the Verilog, EDIF, layout, and wirebonding diagram) is available on the LHEA ACD electronics web page at:

<http://lhea-glast.gsfc.nasa.gov/acd/electronics/#garc>

Appendix 2: GARC Configuration Command Format

The GARC logic core responds only to properly structured commands. There are two possible command types – Trigger Commands and Configuration Commands. Trigger commands initiate an Event Data cycle, causing a GAFE Hold, an analog-to-digital conversion, and the return of an event data packet. Configuration commands are used to either read or write GARC or GAFE registers.

The format for Trigger Commands is detailed in the table below.

Bit(s)	Bit Description	Value
3	Start Bit	1
2:1	Trigger Type Bits	10 for ZS Enabled Trigger 01 for Send All PHA Trigger
0	Parity Bit	Odd parity bit over previous two bits

Therefore, a 1100 is a ZS Enabled Trigger command and a 1010 is a Send All PHA Trigger command.

This format for GARC Configuration Commands is detailed in the table below.

Field	# bits	Function
Start	1	1 for start
CMD Type	2	00 for command
CMD Type Parity	1	Odd Parity over previous 2 bits (without Start bit)
GAFE/GARC Select	1	0 for GARC 1 for GAFE
GAFE/GARC Address	5	GAFE: Select which GAFE, 0x1F for all GAFE GARC: Select which function block
Read/Write	1	0 for write, 1 for read
Data/Dataless	1	0 for dataless, 1 for data, always 1 for ACD
register/function number	4	Which register/function in the function block
CMD Parity	1	Odd parity bit over previous 15 bits
Data	16	Data Field
Data Parity	1	Odd parity bit over previous 16 bits

Appendix 3: GARC Event Data Format

The GARC core returns an event data packet when a valid trigger command is received. The event data format is detailed in the table below.

<u>Field</u>	<u># bits</u>	<u>Function</u>
Start Bit	1	1 for start
Hit Map Bits	18	Bits 17-0 for channels 0-17, bit set if hit in channel
Zero Suppression Bits	18	Bits 17-0 for channels 0-17, bit set if PHA above threshold
CMD/Data ERROR	1	Error in command parity detected
Header Parity	1	Odd parity bit over previous 37 bits
PHA Words (quantity 0-18) Order: Channel 0 to channel 17	15	Bit 14: 1 if another PHA word follows this one, 0 if this is last one Bit 13: 1 for high range, 0 for low range Bits 12-1: the PHA value, 0 to 4095 Bit 0: Odd parity over last 14 bits

Appendix 4: GARC Configuration Data Readback Format

The GARC core returns an register configuration data packet when a valid configuration readback command is received. The configuration readback data format is detailed in the table below.

<u>Field</u>	<u># bits</u>	<u>Function</u>
Start	1	1 for start
GAFE/GARC Select	1	Copy of write command field (0 for GARC, 1 for GAFE)
GAFE/GARC Address	5	Copy of write command field (Select which GAFE)
Read/Write	1	1 for read
Data/Dataless	1	always 1
Register/function number	4	Copy of write command field (which register/function in the function block)
CMD Parity	1	Odd parity bit over previous 12 bits
Data	16	Data, MSB first
CMD/DATA ERROR	1	Error in parity detected
Parity	1	Odd parity bit over previous 17 bits

Appendix 5: MDM Connector Pin List**Connector JHV1 to High Voltage Bias Supply #1**

Connector Pin	Signal Name
JHV1 - 1	HVBS +28V
JHV1 - 2	28V RTN
JHV1 - 3	HV MON P1
JHV1 - 4	DAC P
JHV1 - 5	HV ENABLE 1
JHV1 - 6	HVBS +28V
JHV1 - 7	28V RTN
JHV1 - 8	HV MON N1
JHV1 - 9	DAC N

Connector JHV2 to High Voltage Bias Supply #2

Connector Pin	Signal Name
JHV2 - 1	HVBS +28V
JHV2 - 2	28V RTN
JHV2 - 3	HV MON P2
JHV2 - 4	DAC P
JHV2 - 5	HV ENABLE 2
JHV2 - 6	HVBS +28V
JHV2 - 7	28V RTN
JHV2 - 8	HV MON N2
JHV2 - 9	DAC N

Appendix 6: Series II Circular Connector Pin List

Pin Locations for Connectors JP1 and (JS2)

Signal Name	Function	Connector Pin
ACD_VDD_0A(B)	+3.3V Power to ACD	1
ACD_VDD_1A(B)	+3.3V Power to ACD	3
ACD_VDD_2A(B)	+3.3V Power to ACD	4
ACD_28V_0A(B)	+28V Power to ACD HVBS	5
ACD_28V_1A(B)	+28V Power to ACD HVBS	7
ACD_NVETO_16A(B)P	Veto Ch 16 + to AEM	17
ACD_NVETO_16A(B)M	Veto Ch 16 - to AEM	18
ACD_NVETO_17A(B)P	Veto Ch 17 + to AEM	19
ACD_NVETO_17A(B)M	Veto Ch 17 - to AEM	20
ACD_NCNO_A(B)P	CNO + to AEM	21
ACD_NCNO_A(B)M	CNO - to AEM	22
ACD_HV_AP	High Voltage Supply 1 Monitor + to AEM	23
ACD_HV_AM	High Voltage Supply 1 Monitor - to AEM	24
ACD_TEMP_A(B)P	Temp Monitor + to AEM	25
ACD_TEMP_A(B)M	Temp Monitor - to AEM	26
ACD_HV_BP	High Voltage Supply 2 Monitor + to AEM	27
ACD_HV_BM	High Voltage Supply 2 Monitor - to AEM	28
ACD_GND_0A(B)	+3.3V Power Return	30
ACD_GND_1A(B)	+3.3V Power Return	31
ACD_GND_2A(B)	+3.3V Power Return	32
ACD_28V_RTN_0A(B)	+28V Return	33
ACD_28V_RTN_1A(B)	+28V Return	34
ACD_NVETO_15A(B)M	Veto Ch 15 - to AEM	40
ACD_NVETO_15A(B)P	Veto Ch 15 + to AEM	41
ACD_NVETO_14A(B)M	Veto Ch 14 - to AEM	42
ACD_NVETO_14A(B)P	Veto Ch 14 + to AEM	43
ACD_NVETO_13A(B)M	Veto Ch 13 - to AEM	44
ACD_NVETO_13A(B)P	Veto Ch 13 + to AEM	45
ACD_NVETO_12A(B)M	Veto Ch 12 - to AEM	46
ACD_NVETO_12A(B)P	Veto Ch 12 + to AEM	47
ACD_NVETO_11A(B)M	Veto Ch 11 - to AEM	48
ACD_NVETO_11A(B)P	Veto Ch 11 + to AEM	49
ACD_NVETO_10A(B)M	Veto Ch 10 - to AEM	50
ACD_NVETO_10A(B)P	Veto Ch 10 + to AEM	51
ACD_NVETO_09A(B)M	Veto Ch 9 - to AEM	52
ACD_NVETO_09A(B)P	Veto Ch 9 + to AEM	53
ACD_NVETO_08A(B)M	Veto Ch 8 - to AEM	54
ACD_NVETO_08A(B)P	Veto Ch 8 + to AEM	55
ACD_NVETO_07A(B)M	Veto Ch 7 - to AEM	56

ACD_NVETO_07A(B)P	Veto Ch 7 + to AEM	57
ACD_NVETO_06A(B)M	Veto Ch 6 - to AEM	58
ACD_NVETO_06A(B)P	Veto Ch 6 + to AEM	59
ACD_NVETO_05A(B)M	Veto Ch 5 - to AEM	60
ACD_NVETO_05A(B)P	Veto Ch 5 + to AEM	61
ACD_NVETO_04A(B)M	Veto Ch 4 - to AEM	62
ACD_NVETO_04A(B)P	Veto Ch 4 + to AEM	63
ACD_NVETO_03A(B)M	Veto Ch 3 - to AEM	64
ACD_NVETO_03A(B)P	Veto Ch 3 + to AEM	65
ACD_NVETO_02A(B)M	Veto Ch 2 - to AEM	66
ACD_NVETO_02A(B)P	Veto Ch 2 + to AEM	67
ACD_NVETO_01A(B)M	Veto Ch 1 - to AEM	68
ACD_NVETO_01A(B)P	Veto Ch 1 + to AEM	69
ACD_NVETO_00A(B)M	Veto Ch 0 - to AEM	70
ACD_NVETO_00A(B)P	Veto Ch 0 + to AEM	71
ACD_NSDATA_A(B)M	Data- to AEM	72
ACD_NSDATA_A(B)P	Data+ to AEM	73
ACD_NIRST_A(B)M	Reset- to ACD	74
ACD_NIRST_A(B)P	Reset+ to ACD	75
ACD_NSCMD_A(B)M	Command- to ACD	76
ACD_NSCMD_A(B)P	Command+ to ACD	77
ACD_CLK_A(B)M	Clock- to ACD	78
ACD_CLK_A(B)P	Clock+ to ACD	79
Spare Pins	Pins 8-16, 29, 35-39 not used	rest

Appendix 7: GARC Command Mnemonics and Functions

The following table represents each of the available GARC commands. Additionally, all GAFE commands are passed through the GARC. These command patterns are detailed in the document discussing the GAFE logic. There are two types of GARC commands – trigger commands (4 bits in length) and configuration commands (34 bits in length). The AEM-ACD ICD contains the authoritative formats for all command types, but they are repeated in the appendices of this document for convenience. The table below defines the command mnemonics that will be used in this test.

Note that a GAFE will process a write command either for the address hard-wired to the chip address pins or to an address of 'h1F, the GAFE broadcast address. A GAFE will process a read command only for an address identical to the hard-wired address. It is an operational constraint that, for any given ACD circuit board, each GAFE must have a unique address.

GARC Cmd No.	ACD Command Mnemonic	Rd/Wr Status	Select GARC=0 GAFE=1	Function Block	Register Number	No. of Data Bits	Command Function
1	Trigger_ZS	N/A	N/A	N/A	N/A	N/A	ACD Trigger, Zero-Suppression Enable
2	Trigger_NOZS	N/A	N/A	N/A	N/A	N/A	ACD Trigger, No Zero-Suppression
3	GARC_Reset	W	0	0	1	0	Generates reset for GARC and GAFE registers
4	Veto_Delay_Wr	W	0	0	2	5	Sets Delay from Disc_In to VETO Out
5	Veto_Delay_Rd	R	0	0	2	5	Reads contents of Veto_Delay register
6	GARC_Cal_Strobe	W	0	0	3	0	Sends Calibration Strobe signal to all GAFEs
7	HVBS_Level_Wr	W	0	0	8	12	Sets GARC register value from which HVBS may be commanded in the science mode
8	HVBS_Level_Rd	R	0	0	8	12	Reads contents of HVBS Level register
9	SAA_Level_Wr	W	0	0	9	12	Sets GARC register value from which HVBS may be commanded when in the SAA
10	SAA_Level_Rd	R	0	0	9	12	Reads contents of SAA Level register
11	Use_HV_Normal	W	0	0	10	0	Sends 12 bit value in HVBS Level register to the MAX5121 DAC
12	DAC_HVReg_Rd	R	0	0	10	0	Reads MAX5121 DAC Config Register
13	Use_SAA_Normal	W	0	0	11	0	Sends 12 bit value in SAA Level register to the MAX5121 DAC
14	DAC_SAAReg_Rd	R	0	0	11	0	Reads MAX5121 DAC Config Register
15	Hold_Delay_Wr	W	0	0	12	7	Sets GARC Hold Delay
16	Hold_Delay_Rd	R	0	0	12	7	Reads back value of GARC Hold Delay register
17	Veto_Width_Wr	W	0	0	13	3	Sets width of the VETO signals
18	Veto_Width_Rd	R	0	0	13	3	Reads back width of the VETO width register
19	HitMap_Width_Wr	W	0	0	14	4	Sets width of HitMap pulses
20	HitMap_Width_Rd	R	0	0	14	4	Reads back value in the HitMap width register
21	HitMap_Deptime_Wr	W	0	0	15	3	Sets stretch at end of HitMap pulses
22	HitMap_Deptime_Rd	R	0	0	15	3	Sets stretch at end of HitMap pulses
23	Look_At_Me	W	0	1	4	16	GARC interface selection command (primary/secondary)
24	HitMap_Delay_Wr	W	0	1	8	5	Sets delay from Disc_In to HitMap pulse
25	HitMap_Delay_Rd	R	0	1	8	5	Reads back contents of the HitMap_Delay register
26	PHA_EN0_Wr	W	0	1	9	16	Enables and Disables PHA readout enable, channels 0 -15

27	PHA_EN0_Rd	R	0	1	9	16	Reads back contents of the PHA_EN0 register
28	VETO_EN0_Wr	W	0	1	10	16	Enables and Disables VETO signals, channels 0 -15
29	VETO_EN0_Rd	R	0	1	10	16	Reads back contents of the VETO_EN0 register
30	PHA_EN1_Wr	W	0	1	12	2	Enables and Disables PHA readout enable, channels 16 & 17
31	PHA_EN1_Rd	R	0	1	12	2	Reads back contents of the PHA_EN1 register
32	VETO_EN1_Wr	W	0	1	13	2	Enables and Disables VETO signals, channels 16 & 17
33	VETO_EN1_Rd	R	0	1	13	2	Reads back contents of the VETP_EN1 register
34	Max_PHA_Wr	W	0	1	15	5	Sets the Maximum number (limit) of PHA to be returned in a single event data packet
35	Max_PHA_Rd	R	0	1	15	5	Reads back the contents of the Max_PHA register
36	GARC_Mode_Wr	W	0	2	8	11	Sets values of GARC mode bits
37	GARC_Mode_Rd	R	0	2	8	11	Reads back the value of the GARC mode register
38	GARC_Status	R	0	2	9	6	Reads back the value of the GARC status register
39	GARC_Cmd_Reg	R	0	2	10	16	Reads back the value of the GARC command register
40	GARC_Diagnostic	R	0	2	11	16	Reads back the value of the GARC diagnostic register
41	GARC_Cmd_Rejects	R	0	2	12	8	Reads back the number of rejected commands since reset
42	FREE_Board_ID	R	0	2	13	8	Reads back the FREE board serial number
43	GARC_Version	R	0	2	14	3	Reads back the GARC ASIC version number
44	PHA_Thresh00_Wr	W	0	3	8	12	Writes PHA ZS threshold for channel 00
45	PHA_Thresh00_Rd	R	0	3	8	12	Reads back PHA ZS threshold register for channel 00
46	PHA_Thresh01_Wr	W	0	3	9	12	Writes PHA ZS threshold for channel 01
47	PHA_Thresh01_Rd	R	0	3	9	12	Reads back PHA ZS threshold register for channel 01
48	PHA_Thresh02_Wr	W	0	3	10	12	Writes PHA ZS threshold for channel 02
49	PHA_Thresh02_Rd	R	0	3	10	12	Reads back PHA ZS threshold register for channel 02
50	PHA_Thresh03_Wr	W	0	3	11	12	Writes PHA ZS threshold for channel 03
51	PHA_Thresh03_Rd	R	0	3	11	12	Reads back PHA ZS threshold register for channel 03
52	PHA_Thresh04_Wr	W	0	3	12	12	Writes PHA ZS threshold for channel 04
53	PHA_Thresh04_Rd	R	0	3	12	12	Reads back PHA ZS threshold register for channel 04
54	PHA_Thresh05_Wr	W	0	3	13	12	Writes PHA ZS threshold for channel 05
55	PHA_Thresh05_Rd	R	0	3	13	12	Reads back PHA ZS threshold register for channel 05
56	PHA_Thresh06_Wr	W	0	3	14	12	Writes PHA ZS threshold for channel 06
57	PHA_Thresh06_Rd	R	0	3	14	12	Reads back PHA ZS threshold register for channel 06
58	PHA_Thresh07_Wr	W	0	4	8	12	Writes PHA ZS threshold for channel 07
59	PHA_Thresh07_Rd	R	0	4	8	12	Reads back PHA ZS threshold register for channel 07
60	PHA_Thresh08_Wr	W	0	4	9	12	Writes PHA ZS threshold for channel 08
61	PHA_Thresh08_Rd	R	0	4	9	12	Reads back PHA ZS threshold register for channel 08
62	PHA_Thresh09_Wr	W	0	4	10	12	Writes PHA ZS threshold for channel 09
63	PHA_Thresh09_Rd	R	0	4	10	12	Reads back PHA ZS threshold register

							for channel 09
64	PHA_Thresh10_Wr	W	0	4	11	12	Writes PHA ZS threshold for channel 10
65	PHA_Thresh10_Rd	R	0	4	11	12	Reads back PHA ZS threshold register for channel 10
66	PHA_Thresh11_Wr	W	0	4	12	12	Writes PHA ZS threshold for channel 11
67	PHA_Thresh11_Rd	R	0	4	12	12	Reads back PHA ZS threshold register for channel 11
68	PHA_Thresh12_Wr	W	0	4	13	12	Writes PHA ZS threshold for channel 12
69	PHA_Thresh12_Rd	R	0	4	13	12	Reads back PHA ZS threshold register for channel 12
70	PHA_Thresh13_Wr	W	0	4	14	12	Writes PHA ZS threshold for channel 13
71	PHA_Thresh13_Rd	R	0	4	14	12	Reads back PHA ZS threshold register for channel 13
72	PHA_Thresh14_Wr	W	0	5	8	12	Writes PHA ZS threshold for channel 14
73	PHA_Thresh14_Rd	R	0	5	8	12	Reads back PHA ZS threshold register for channel 14
74	PHA_Thresh15_Wr	W	0	5	9	12	Writes PHA ZS threshold for channel 15
75	PHA_Thresh15_Rd	R	0	5	9	12	Reads back PHA ZS threshold register for channel 15
76	PHA_Thresh16_Wr	W	0	5	10	12	Writes PHA ZS threshold for channel 16
77	PHA_Thresh16_Rd	R	0	5	10	12	Reads back PHA ZS threshold register for channel 16
78	PHA_Thresh17_Wr	W	0	5	11	12	Writes PHA ZS threshold for channel 17
79	PHA_Thresh17_Rd	R	0	5	11	12	Reads back PHA ZS threshold register for channel 17
80	ADC_TACQ_Wr	W	0	5	12	6	Sets ADC Acquisition Time from Hold to Start of Conversion
81	ADC_TACQ_Rd	R	0	5	12	6	Reads back contents of the ADC_TACQ register
82	GAFE_Mode_Wr	W	1	GAFE Addr	0	16	Writes the GAFE mode register for the ASIC addressed
83	GAFE_Mode_Rd	R	1	GAFE Addr	0	16	Reads the GAFE mode register contents for the ASIC addressed
84	GAFE_VETO_Wr	W	1	GAFE Addr	1	6	Writes the DAC1 register in the GAFE addressed
85	GAFE_VETO_Rd	R	1	GAFE Addr	1	6	Reads back the contents of the DAC1 register in the addressed GAFE
86	GAFE_VERNIER_Wr	W	1	GAFE Addr	2	6	Writes the DAC2 register in the GAFE addressed
87	GAFE_VERNIER_Rd	R	1	GAFE Addr	2	6	Reads back the contents of the DAC2 register in the addressed GAFE
88	GAFE_HLD_Wr	W	1	GAFE Addr	3	6	Writes the DAC3 register in the GAFE addressed
89	GAFE_HLD_Rd	R	1	GAFE Addr	3	6	Reads back the contents of the DAC3 register in the addressed GAFE
90	GAFE_BIAS_Wr	W	1	GAFE Addr	4	6	Writes the DAC4 register in the GAFE addressed
91	GAFE_BIAS_Rd	R	1	GAFE Addr	4	6	Reads back the contents of the DAC4 register in the addressed GAFE
92	GAFE_TCI_Wr	W	1	GAFE Addr	5	6	Writes the DAC5 register in the GAFE addressed
93	GAFE_TCI_Rd	R	1	GAFE Addr	5	6	Reads back the contents of the DAC5 register in the addressed GAFE
94	GAFE_Version	R	1	GAFE Addr	6	3	Reads back the GAFE ASIC version
95	GAFE_Write_Ctr	R	1	GAFE Addr	7	8	Reads back the contents of the GAFE write counter register
96	GAFE_Reject_Ctr	R	1	GAFE Addr	8	8	Reads back the contents of the GAFE command reject register
97	GAFE_Cmd_Ctr	R	1	GAFE Addr	9	8	Reads back the contents of the GAFE command counter
98	GAFE_Chip_Addr	R	1	GAFE Addr	10	5	Reads back the hardwired address of a GAFE ASIC

Appendix 8: Test Results Record

All measurements and test results will be recorded in this Test Results Record. A copy of the entire this entire document is not required each time the test is performed. The appendix will serve as the official record each time this test is performed.

3.0 QA Signoff

Quality Assurance approval to proceed with the test - _____

(NOTE: If QA gives verbal approval to proceed but is not in attendance for the test, record the date and the time of approval.)

3.1 FREE Assembly Identification

Chamber Temperature: _____

The test conductor for this test is: _____

Date of Test: _____

The serial number of the FREE card assembly is: _____

The identification/Serial Number listed on the GARC ASIC is: _____

The identification/Serial Numbers listed on the GAFE ASICs are:

GAFE Channel	ASIC Serial Number
0	
1	
2	
3	
4	
5	
6	
7	
8	
9	
10	
11	
12	
13	
14	
15	
16	
17	

3.2 Test Equipment Utilized

Instrument Type	Manufacturer & Model Number	NASA ID Number	Calibration Due Date
Power Supply for FREE & GSE +3.3V & +5.0V			
Multimeter 1			
Multimeter 2			
Oscilloscope			
Pulse Generator			
Tail Pulse Generator			
Charge Terminator Box			
Temperature Sensor			

3.3 Chassis Ground verification

Ground verified - _____

4.1 Verification of Proper LVDS Terminations

Test is looking into the GSE.

Test Omitted - _____

Measurement No.	Signal Pair	Pin 1	Pin 2	Expected Resistance	Verified
1	ACD_NVETO_16_A	JP1 - 17	JP1 - 18	95 Ω < R < 105 Ω	
2	ACD_NVETO_17_A	JP1 - 19	JP1 - 20	95 Ω < R < 105 Ω	
3	ACD_CNO_A	JP1 - 21	JP1 - 22	95 Ω < R < 105 Ω	
4	ACD_NVETO_15_A	JP1 - 40	JP1 - 41	95 Ω < R < 105 Ω	
5	ACD_NVETO_14_A	JP1 - 42	JP1 - 43	95 Ω < R < 105 Ω	
6	ACD_NVETO_13_A	JP1 - 44	JP1 - 45	95 Ω < R < 105 Ω	

7	ACD_NVETO_12_A	JP1 - 46	JP1 - 47	95 Ω < R < 105 Ω	
8	ACD_NVETO_11_A	JP1 - 48	JP1 - 49	95 Ω < R < 105 Ω	
9	ACD_NVETO_10_A	JP1 - 50	JP1 - 51	95 Ω < R < 105 Ω	
10	ACD_NVETO_09_A	JP1 - 52	JP1 - 53	95 Ω < R < 105 Ω	
11	ACD_NVETO_08_A	JP1 - 54	JP1 - 55	95 Ω < R < 105 Ω	
12	ACD_NVETO_07_A	JP1 - 56	JP1 - 57	95 Ω < R < 105 Ω	
13	ACD_NVETO_06_A	JP1 - 58	JP1 - 59	95 Ω < R < 105 Ω	
14	ACD_NVETO_05_A	JP1 - 60	JP1 - 61	95 Ω < R < 105 Ω	
15	ACD_NVETO_04_A	JP1 - 62	JP1 - 63	95 Ω < R < 105 Ω	
16	ACD_NVETO_03_A	JP1 - 64	JP1 - 65	95 Ω < R < 105 Ω	
17	ACD_NVETO_02_A	JP1 - 66	JP1 - 67	95 Ω < R < 105 Ω	
18	ACD_NVETO_01_A	JP1 - 68	JP1 - 69	95 Ω < R < 105 Ω	
19	ACD_NVETO_00_A	JP1 - 70	JP1 - 71	95 Ω < R < 105 Ω	
20	ACD_NSDATA_A	JP1 - 72	JP1 - 73	95 Ω < R < 105 Ω	
21	ACD_NRST_A	JP1 - 74	JP1 - 75	R > 100 kΩ	
22	ACD_NSCMD_A	JP1 - 76	JP1 - 77	R > 100 kΩ	
23	ACD_CLK_A	JP1 - 78	JP1 - 79	R > 100 kΩ	
24	ACD_NVETO_16_B	JS2 - 17	JS2 - 18	95 Ω < R < 105 Ω	
25	ACD_NVETO_17_B	JS2 - 19	JS2 - 20	95 Ω < R < 105 Ω	
26	ACD_CNO_B	JS2 - 21	JS2 - 22	95 Ω < R < 105 Ω	
27	ACD_NVETO_15_B	JS2 - 40	JS2 - 41	95 Ω < R < 105 Ω	
28	ACD_NVETO_14_B	JS2 - 42	JS2 - 43	95 Ω < R < 105 Ω	
29	ACD_NVETO_13_B	JS2 - 44	JS2 - 45	95 Ω < R < 105 Ω	
30	ACD_NVETO_12_B	JS2 - 46	JS2 - 47	95 Ω < R < 105 Ω	
31	ACD_NVETO_11_B	JS2 - 48	JS2 - 49	95 Ω < R < 105 Ω	
32	ACD_NVETO_10_B	JS2 - 50	JS2 - 51	95 Ω < R < 105 Ω	
33	ACD_NVETO_09_B	JS2 - 52	JS2 - 53	95 Ω < R < 105 Ω	
34	ACD_NVETO_08_B	JS2 - 54	JS2 - 55	95 Ω < R < 105 Ω	
35	ACD_NVETO_07_B	JS2 - 56	JS2 - 57	95 Ω < R < 105 Ω	
36	ACD_NVETO_06_B	JS2 - 58	JS2 - 59	95 Ω < R < 105 Ω	
37	ACD_NVETO_05_B	JS2 - 60	JS2 - 61	95 Ω < R < 105 Ω	
38	ACD_NVETO_04_B	JS2 - 62	JS2 - 63	95 Ω < R < 105 Ω	
39	ACD_NVETO_03_B	JS2 - 64	JS2 - 65	95 Ω < R < 105 Ω	
40	ACD_NVETO_02_B	JS2 - 66	JS2 - 67	95 Ω < R < 105 Ω	
41	ACD_NVETO_01_B	JS2 - 68	JS2 - 69	95 Ω < R < 105 Ω	
42	ACD_NVETO_00_B	JS2 - 70	JS2 - 71	95 Ω < R < 105 Ω	
43	ACD_NSDATA_B	JS2 - 72	JS2 - 73	95 Ω < R < 105 Ω	
44	ACD_NRST_B	JS2 - 74	JS2 - 75	R > 100 kΩ	
45	ACD_NSCMD_B	JS2 - 76	JS2 - 77	R > 100 kΩ	
46	ACD_CLK_B	JS2 - 78	JS2 - 79	R > 100 kΩ	

4.2 Stray Voltage Test at the AEM Interface

Test is looking into the GSE with JP1-30 as the ground return.

Test Omitted - _____

Meas. No.	AEM Interface Pin	Signal Name	Expected Voltage	Measured Voltage
1	JP1 - 1	ACD_VDD_0A	+3.3V	
2	JP1 - 3	ACD_VDD_1A	+3.3V	

3	JP1 - 4	ACD_VDD_2A	+3.3V	
4	JP1 - 5	ACD_28V_0A	+28V	
5	JP1 - 7	ACD_28V_1A	+28V	
6	JP1 - 17	ACD_NVETO_16AP	0 < V < 3.3	
7	JP1 - 18	ACD_NVETO_16AM	0 < V < 3.3	
8	JP1 - 19	ACD_NVETO_17AP	0 < V < 3.3	
9	JP1 - 20	ACD_NVETO_17AM	0 < V < 3.3	
10	JP1 - 21	ACD_NCNO_AP	0 < V < 3.3	
11	JP1 - 22	ACD_NCNO_AM	0 < V < 3.3	
12	JP1 - 23	ACD_HV_AP	0 < V < 3.3	
13	JP1 - 24	ACD_HV_AM	0 < V < 3.3	
14	JP1 - 25	ACD_TEMP_AP	0	
15	JP1 - 26	ACD_TEMP_AM	0	
17	JP1 - 31	ACD_GND_1A	0	
18	JP1 - 32	ACD_GND_2A	0	
19	JP1 - 33	ACD_28V_RTN_0A	0	
20	JP1 - 34	ACD_28V_RTN_1A	0	
21	JP1 - 40	ACD_NVETO_15AM	V < 200mV	
22	JP1 - 41	ACD_NVETO_15AP	V < 200mV	
23	JP1 - 42	ACD_NVETO_14AM	V < 200mV	
24	JP1 - 43	ACD_NVETO_14AP	V < 200mV	
25	JP1 - 44	ACD_NVETO_13AM	V < 200mV	
26	JP1 - 45	ACD_NVETO_13AP	V < 200mV	
27	JP1 - 46	ACD_NVETO_12AM	V < 200mV	
28	JP1 - 47	ACD_NVETO_12AP	V < 200mV	
29	JP1 - 48	ACD_NVETO_11AM	V < 200mV	
31	JP1 - 50	ACD_NVETO_10AM	V < 200mV	
32	JP1 - 51	ACD_NVETO_10AP	V < 200mV	
33	JP1 - 52	ACD_NVETO_09AM	V < 200mV	
34	JP1 - 53	ACD_NVETO_09AP	V < 200mV	
35	JP1 - 54	ACD_NVETO_08AM	V < 200mV	
36	JP1 - 55	ACD_NVETO_08AP	V < 200mV	
37	JP1 - 56	ACD_NVETO_07AM	V < 200mV	
38	JP1 - 57	ACD_NVETO_07AP	V < 200mV	
39	JP1 - 58	ACD_NVETO_06AM	V < 200mV	
40	JP1 - 59	ACD_NVETO_06AP	V < 200mV	
41	JP1 - 60	ACD_NVETO_05AM	V < 200mV	
42	JP1 - 61	ACD_NVETO_05AP	V < 200mV	
43	JP1 - 62	ACD_NVETO_04AM	V < 200mV	
44	JP1 - 63	ACD_NVETO_04AP	V < 200mV	
45	JP1 - 64	ACD_NVETO_03AM	V < 200mV	
46	JP1 - 65	ACD_NVETO_03AP	V < 200mV	
47	JP1 - 66	ACD_NVETO_02AM	V < 200mV	
48	JP1 - 67	ACD_NVETO_02AP	V < 200mV	
49	JP1 - 68	ACD_NVETO_01AM	V < 200mV	
50	JP1 - 69	ACD_NVETO_01AP	V < 200mV	
51	JP1 - 70	ACD_NVETO_00AM	V < 200mV	
52	JP1 - 71	ACD_NVETO_00AP	V < 200mV	
53	JP1 - 72	ACD_NSDATA_AM	V < 200mV	
54	JP1 - 73	ACD_NSDATA_AP	V < 200mV	
55	JP1 - 74	ACD_NRST_AM	V < 200mV	

56	JP1 - 75	ACD_NRST_AP	V > 2.3V	
57	JP1 - 76	ACD_NSCMD_AM	V < 200mV	
58	JP1 - 77	ACD_NSCMD_AP	V > 2.3V	
59	JP1 - 78	ACD_CLK_AM	1.1V < V < 1.5V	
60	JP1 - 79	ACD_CLK_AP	1.1V < V < 1.5V	
61	JS2 - 1	ACD_VDD_0B	+3.3V	
62	JS2 - 3	ACD_VDD_1B	+3.3V	
63	JS2 - 4	ACD_VDD_2B	+3.3V	
64	JS2 - 5	ACD_28V_0B	+28V	
65	JS2 - 7	ACD_28V_1B	+28V	
66	JS2 - 17	ACD_NVETO_16BP	V < 200mV	
67	JS2 - 18	ACD_NVETO_16BM	V < 200mV	
68	JS2 - 19	ACD_NVETO_17BP	V < 200mV	
69	JS2 - 20	ACD_NVETO_17BM	V < 200mV	
70	JS2 - 21	ACD_NCNO_BP	V < 200mV	
71	JS2 - 22	ACD_NCNO_BM	V < 200mV	
72	JS2 - 23	ACD_HV_BP	V < 200mV	
73	JS2 - 24	ACD_HV_BM	V < 200mV	
74	JS2 - 25	ACD_TEMP_BP	0	
75	JS2 - 26	ACD_TEMP_BM	0	
76	JS2 - 30	ACD_GND_0B	0	
77	JS2 - 31	ACD_GND_1B	0	
78	JS2 - 32	ACD_GND_2B	0	
79	JS2 - 33	ACD_28V_RTN_0B	0	
80	JS2 - 34	ACD_28V_RTN_1B	0	
81	JS2 - 40	ACD_NVETO_15BM	V < 200mV	
82	JS2 - 41	ACD_NVETO_15BP	V < 200mV	
83	JS2 - 42	ACD_NVETO_14BM	V < 200mV	
84	JS2 - 43	ACD_NVETO_14BP	V < 200mV	
85	JS2 - 44	ACD_NVETO_13BM	V < 200mV	
86	JS2 - 45	ACD_NVETO_13BP	V < 200mV	
87	JS2 - 46	ACD_NVETO_12BM	V < 200mV	
88	JS2 - 47	ACD_NVETO_12BP	V < 200mV	
89	JS2 - 48	ACD_NVETO_11BM	V < 200mV	
90	JS2 - 49	ACD_NVETO_11BP	V < 200mV	
91	JS2 - 50	ACD_NVETO_10BM	V < 200mV	
92	JS2 - 51	ACD_NVETO_10BP	V < 200mV	
93	JS2 - 52	ACD_NVETO_09BM	V < 200mV	
94	JS2 - 53	ACD_NVETO_09BP	V < 200mV	
95	JS2 - 54	ACD_NVETO_08BM	V < 200mV	
96	JS2 - 55	ACD_NVETO_08BP	V < 200mV	
97	JS2 - 56	ACD_NVETO_07BM	V < 200mV	
98	JS2 - 57	ACD_NVETO_07BP	V < 200mV	
99	JS2 - 58	ACD_NVETO_06BM	V < 200mV	
100	JS2 - 59	ACD_NVETO_06BP	V < 200mV	
101	JS2 - 60	ACD_NVETO_05BM	V < 200mV	
102	JS2 - 61	ACD_NVETO_05BP	V < 200mV	
103	JS2 - 62	ACD_NVETO_04BM	V < 200mV	
104	JS2 - 63	ACD_NVETO_04BP	V < 200mV	
105	JS2 - 64	ACD_NVETO_03BM	V < 200mV	
106	JS2 - 65	ACD_NVETO_03BP	V < 200mV	

107	JS2 - 66	ACD_NVETO_02BM	V < 200mV	
108	JS2 - 67	ACD_NVETO_02BP	V < 200mV	
109	JS2 - 68	ACD_NVETO_01BM	V < 200mV	
110	JS2 - 69	ACD_NVETO_01BP	V < 200mV	
111	JS2 - 70	ACD_NVETO_00BM	V < 200mV	
112	JS2 - 71	ACD_NVETO_00BP	V < 200mV	
113	JS2 - 72	ACD_NSDATA_BM	V < 200mV	
114	JS2 - 73	ACD_NSDATA_BP	V < 200mV	
115	JS2 - 74	ACD_NRST_BM	V < 200mV	
116	JS2 - 75	ACD_NRST_BP	V > 2.3V	
117	JS2 - 76	ACD_NSCMD_BM	V < 200mV	
118	JS2 - 77	ACD_NSCMD_BP	V > 2.3V	
119	JS2 - 78	ACD_CLK_BM	1.1V < V < 1.5V	
120	JS2 - 79	ACD_CLK_BP	1.1V < V < 1.5V	

5.1 GARC and GAFE Registers Initial Reset Test

Chamber Temperature - _____

Temperature of FREE Board - _____

Temperature of GARC - _____

+3.3V Current - _____

Turn On reset verified - _____

FREE Board ID - _____

Reset Command verified - _____

5.2 GARC/GAFE Register Read/Write Tests

Test Completed - _____

5.3 FREE Power Measurement at the Nominal Power Supply Voltage

GARC Mode	GARC_Mode_Wr Data Argument	+3.0V Current Measured (mA)	+3.0V Current Expected (mA)
LVDS "A" Drivers Enabled LVDS "B" Drivers Enabled	768		170 ± 10mA
LVDS "A" Drivers Enabled LVDS "B" Drivers Disabled	256		125 ± 10mA
LVDS "A" Drivers Disabled LVDS "B" Drivers Enabled	512		125 ± 10mA
LVDS "A" Drivers Disabled LVDS "B" Drivers Disabled	0		75 ± 10mA

5.4 FREE Power Measurement at the Minimum Power Supply Voltage

GARC Mode	GARC_Mode_Wr Data Argument	+3.0V Current Measured (mA)	+3.0V Current Expected (mA)
LVDS "A" Drivers Enabled LVDS "B" Drivers Enabled	768		170 ± 10mA
LVDS "A" Drivers Enabled LVDS "B" Drivers Disabled	256		125 ± 10mA
LVDS "A" Drivers Disabled LVDS "B" Drivers Enabled	512		125 ± 10mA
LVDS "A" Drivers Disabled LVDS "B" Drivers Disabled	0		75 ± 10mA

5.5 FREE Power Measurement at the Maximum Power Supply Voltage

GARC Mode	GARC_Mode_Wr Data Argument	+3.6V Current Measured (mA)	+3.6V Current Expected (mA)
LVDS "A" Drivers Enabled LVDS "B" Drivers Enabled	768		230 ± 10mA
LVDS "A" Drivers Enabled LVDS "B" Drivers Disabled	256		175 ± 10mA
LVDS "A" Drivers Disabled LVDS "B" Drivers Enabled	512		175 ± 10mA
LVDS "A" Drivers Disabled LVDS "B" Drivers Disabled	0		115 ± 10mA

5.6 Test of the Look-At-Me Circuitry

This test may be automated using the LabView GSE via the GARC Look At Me Test.txt script

Test Completed - _____

5.7 HVBS DAC Test

This test may be automated using the LabView GSE via the GARC HVBS DAC Level Test.txt script

Meas. No.	DAC SETTING	JHV1-4 to JHV1-9 (HV-DAC)
1	0	
2	200	
3	400	
4	600	
5	800	
6	1000	
7	1200	
8	1400	
9	1600	
10	1800	

11	2000	
12	2200	
13	2400	
14	2600	
15	2800	
16	3000	
17	3200	
18	3400	
19	3600	
20	3800	
21	4000	
22	4095	

5.8 Test of the HVBS Triple Modular Redundancy Circuitry

This test may be automated using the LabView GSE via the GARC HV Enable Test.tst script. Ground return is at the power supply.

Voltage at JHV1-5 when Enabled - _____(3.7V)

Voltage at JHV2-5 when Enabled - _____(3.7V)

Voltage at JHV1-5 when Disabled - _____(0.04V)

Voltage at JHV2-5 when Disabled - _____(0.04V)

Test Completed - _____

5.9 FREE Circuit Assembly Characterization Tests

Characterization of each of the 18 GAFE chips

Run script _____

Data file name: _____

All printouts are to be attached to the Test Results Record.

5.10 GAFE Baseline PHA Test

GAFE Channel	GAFE ADC Baseline (Channel number)
0	
1	
2	

3	
4	
5	
6	
7	
8	
9	
10	
11	
12	
13	
14	
15	
16	
17	

5.11 Multiple System Clock Speed Test at +3.0V and +3.6V

+3.0V current - _____

Clock Frequency set to 22MHz

Register Test Complete - _____

DAC Checkout

This test may be automated using the LabView GSE via the GARC HVBS DAC Level Test.txt script.

Meas. No.	DAC SETTING	JHV1-4 to JHV1-9 (HV-DAC)
1	0	
2	1000	
3	2000	
4	3000	
5	4000	
6	4095	

+3.6V current - _____

Register Test Complete - _____

DAC Checkout

This test may be automated using the LabView GSE via the GARC HVBS DAC Level Test.txt script.

Meas. No.	DAC SETTING	JHV1-4 to JHV1-9 (HV-DAC)
1	0	
2	1000	
3	2000	
4	3000	

5	4000	
6	4095	

Clock Frequency set to 14MHz

Register Test Complete - _____

DAC Checkout

This test may be automated using the LabView GSE via the GARC HVBS DAC Level Test.txt script.

Meas. No.	DAC SETTING	JHV1-4 to JHV1-9 (HV-DAC)
1	0	
2	1000	
3	2000	
4	3000	
5	4000	
6	4095	

Set the power supply to +3.0V.

Register Test Complete - _____

DAC Checkout

This test may be automated using the LabView GSE via the GARC HVBS DAC Level Test.txt script.

Meas. No.	DAC SETTING	JHV1-4 to JHV1-9 (HV-DAC)
1	0	
2	1000	
3	2000	
4	3000	
5	4000	
6	4095	

5.12 Power Supply Rail Tests – 3.0V to 3.6V

Voltage set to +3.0V

Characterization of each of the 18 GAFE chips

Run script _____

Data file used: _____

All printouts are to be attached to the Test Results Record.

Voltage set to +3.6V

Characterization of each of the 18 GAFE chips

Run script _____

Data file used: _____

All printouts are to be attached to the Test Results Record.

This completes the Test.