

To: D. Thompson
From: D. Sheppard
Re: GLAST LAT ACD FREE Electronics Problem Report ACD-0-001
Date: 2-11-2004
Cc: R. Baker, J. Odom, M. Smith, G. Unger, G. Haller

Summary:

On 1/15/04, a Problem Report was written against the ACD electronics. This references a problem with uninitialized flip-flops in the GARC V3 ASIC. A solution is proposed that involves wire-Oring the clock and reset signals on the FREE printed circuit board and adding terminations resistors on the DAQ side of the interface.

Description of the Condition Referenced in the Original Problem Report:

On January 15, 2004, the day after GARC laser testing at NRL, a Problem Report was issued against the ACD electronics to detail a power-up anomaly on the FREE prototype board.

This report (available via https://gprs.gsfc.nasa.gov/prpfr/frontmenu_dsp.cfm) stated the problem as follows:

This problem relates to a potential problem during GARC power up. This description is based on work observed in the lab by Baker, Odom, and Sheppard in multiple test setups. A mode has been found where the GARC does not initialize properly. Specifically, when the GARC is powered up after the GARC test board voltage is clamped to 0.0 volts, the GARC is in a non operational mode with the GAFE_RESET and NDAC_CLR lines asserted. This indicates that the GARC is held in the reset mode. A switch to B (redundant) side is required to restore operations. The hypothesis is that the reset flip-flops power up in the "on" state and that clocks on both A and B side are required to clear them. These flip-flops are used in the reset "deglitch" circuitry and do not have explicit resets themselves. Therefore, the start-up configuration of these flip-flops is not determinant. When the test board is not operated in a mode that the GARC voltage is clamped to 0.0V, it appears that the GSE board partially powers the GARC circuitry via protection diodes near the LVDS receivers. In this mode, the GARC appears to start up correctly. A non-operational power up mode may also happen when the GSE is powered up first, then the GARC test board is powered up; this has been observed in the lab. We will need to test FREE cards with the flight-like G3 GSE to evaluate the overall susceptibility of the ACD electronics in that configuration. This condition has been observed during the GARC V3 laser radiation test at the Naval Research Laboratory on 1-14-04. We believe that the laser radiation was able to toggle the state of one of the reset flip-flops, causing the GARC to enter this condition. We also believe that this condition was replicated with a photo-flash test performed on an exposed GARC V3 die in Bob Baker's lab.

Information Acquired Since the Submission of the Problem Report:

The problem has been investigated further since the original Problem Report. Several modes of interface combinations have been tested and some show susceptibility to an incorrect startup mode. Specifically, to make the tests more flight like, two GSE boards have been modified to test the simulated-GASU drivers in the powered-on-enable mode, the powered-on-disabled mode, and the power-off mode and to allow testing of these conditions on both the primary and secondary channels. This is a higher fidelity test environment than previously existed. Testing in Bob Baker's lab confirmed the potential of a stuck-at-reset mode. This condition could be cleared by either power-cycling or application of a system clock. There were times that more than one power cycle was required to clear a stuck-at-reset condition.

It has been determined that there is a requirement to take action and implement a problem resolution that will be appropriate for a flight system.

Discussion of a Solution:

Initially, there are at least three solution paths that appear to be available:

1. Design, fabricate, and test a new GARC ASIC (this would be GARC V4)
2. Design, fabricate, and test new FREE flight printed circuit boards that incorporate new circuitry to provide a fix
3. Modify the existing boards and cabling to implement a solution.

Some of the considerations for each of these possibilities are discussed below.

Choice of Solution Paths:

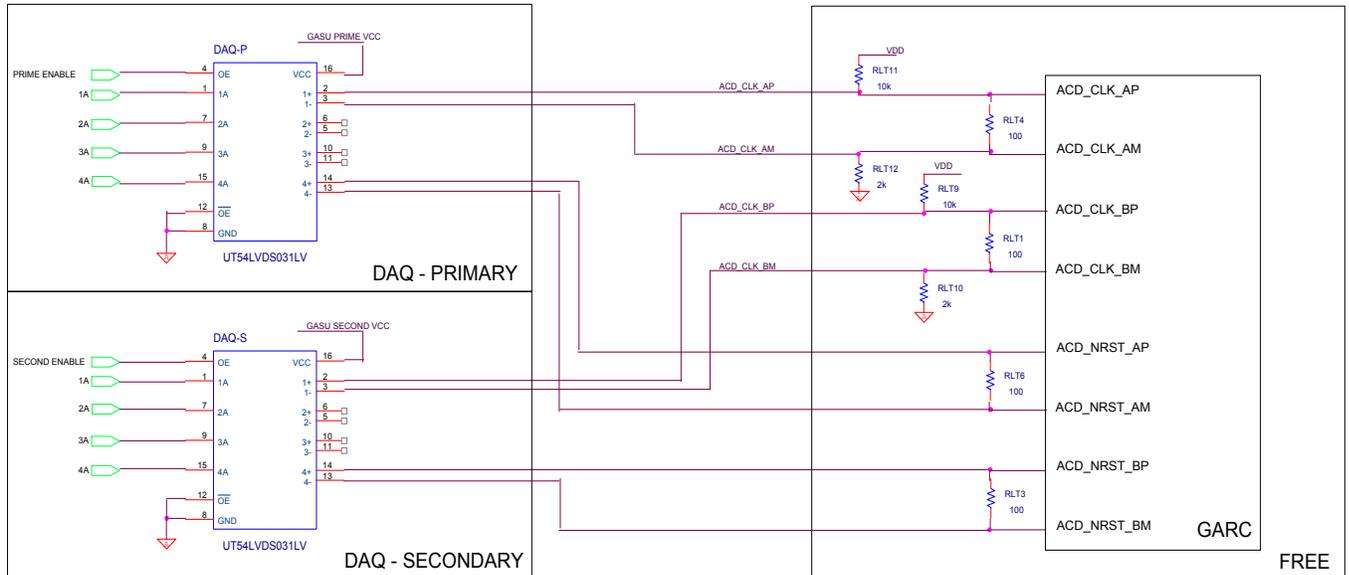
Over the past several days, these options were discussed with several of the engineers at GSFC. A variety of approaches were considered. The approaches detailed below are presented for consideration. The third approach (the wired-OR) is the favored approach for the electronics team based on circuit functionality, circuit reliability, and mechanical volume restrictions.

Solution 1: The best and cleanest solution from a technical perspective would be to produce a new version of the GARC ASIC. However, this would cost many tens of thousands of dollars and require 4-6 months of schedule time. Due to these constraints, this path seems unworkable unless no other solution may be found (but it is presented as an available option).

Solution 2: Another solution would be to modify all the present flight printed circuit cards and add new circuitry to mitigate the problem on-board outside the present GARC V3 ASIC. This would involve adding two discrete LVDS receivers (UT54LVDS032LV), two discrete logic gates, and two discrete driver ICs (UT54LVDS031LV) to the FREE card. The two clocks (prime and redundant), the two command data (prime and redundant), and the two reset lines (prime and redundant) would each be received differentially and converted to single-ended signals. The three signal groups would be logically OR'd. It is critical to do the same operation to the incoming command data as to the clocks in this approach. If this is not done, there will be a major timing skew between the incoming clock and the incoming data. These single-ended OR'd signals would be input to differential drivers, which would in turn drive the GARC receivers. The advantage to this solution would be that there would be no physical OR configuration and no added components in the DAQ. The disadvantage would be that it will be more difficult (and possibly more costly if new boards are required) to implement.

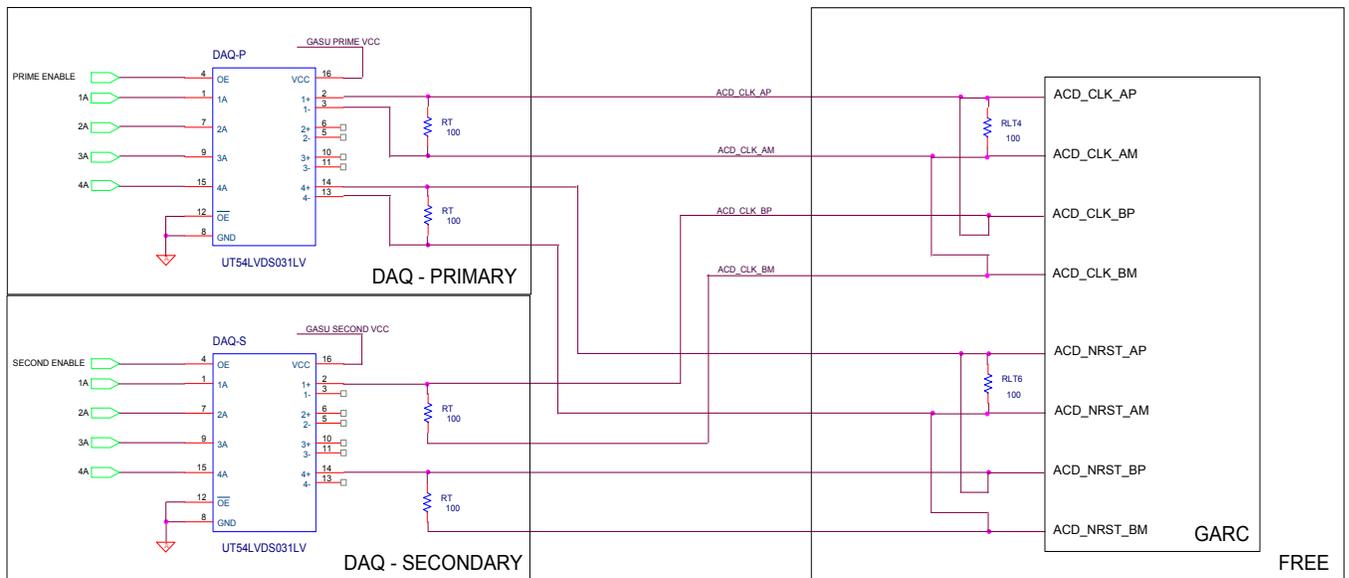
Solution 3: This would be a fix involving wire-ORing the primary and redundant driver circuits. This would involve changing from the present circuit, which is shown in the schematic below,

Present Circuit



to the proposed circuit shown at the bottom of the page. This involves removing termination resistors on the FREE board and adding termination resistors on the DAQ interface board, as drawn.

Proposed Circuit



The modifications to the FREE card involve the following:

1. Removing secondary side termination resistor RLT1
2. Wire ACD_CLK_BP to ACD_CLK_AP on the FREE card with a 30 gauge wire. This is a short wire of less than one inch.
3. Similarly, wire ACD_CLK_BM to ACD_CLK_AM on the FREE card with a 30 gauge wire. This is also a short wire of less than one inch.
4. Disconnect RLT11 from ACD_CLK_AP (removing the 10k pullup)
5. Disconnect RLT12 from ACD_CLK_AM (removing the 2k pulldown)
6. Disconnect RLT9 from ACD_CLK_BP (removing the 10k pullup)
7. Disconnect RLT10 from ACD_CLK_BM (removing the 2k pulldown)
8. Remove secondary side termination resistor RLT3
9. Wire ACD_NRST_BP to ACD_NRST_AP
10. Wire ACD_NRST_BM to ACD_NRST_AM

The modifications to each DAQ FREE card channel would be:

1. Add a termination resistor across the ACD_CLK_P and ACD_CLK_M signals.
2. Add a termination resistor across the ACD_NRST_P and ACD_NRST_M signals

The four resistors, RLT9-RLT12, were originally placed at the inputs of the GARC LVDS receivers. This was to mitigate a known problem of the GARC receivers “chattering” (or switching on reflections/random system noise) when not driven from a powered driver. This was originally implemented on the breadboard FREE cards to eliminate the problem of spurious resets being detected by chattering clock circuitry on the unterminated side. Flowing a relatively small current (e.g., < 300 uA) through the GARC LVDS termination resistor has stabilized these inputs during testing. This is one area where the functionality of the custom-designed LVDS receivers depart from the LVDS standard. Since both primary and redundant reset circuits will now be continually clocked, it is important to prevent the “chattering” of the unpowered NRESET receiver inputs. This is accomplished by replicating the clock driver wire-OR on the ACD_NRST inputs as shown in the schematic above.

This approach has been reviewed by engineers closely involved with a similar situation on the Swift/BAT program. The point was made that it is critical to ensure that the DAQ drivers and receivers on the unpowered board in the GASU contain cold-spares buffers; without this, there is the potential for an additional interface problem. Checking the DAQ parts list (from N. Virmani, 12-30-03), the part numbers listed are UT54LVDS031LV and UT54LVDS032LV. Both of these part numbers do in fact have the correct cold-spares buffer interface. This ensures that a powered LVDS driver can drive the termination resistor on an unpowered LVDS receiver without creating an inadvertent sneak-current path through the powered-off board (as seen on the Swift program). The final test of the FREE card interface will be with the flight-like engineering model GASU, but it seems at first glance that the interface approach is correct.

Simulations of the Flight GARC Receiver Schematic (courtesy M.Smith):

In addition to giving advice based on the experience of Swift/BAT LVDS signal integrity investigations, Miles Smith has performed simulations of the GARC receiver design. He has found that the minimum switching voltage at 24 MHz (i.e., 20 MHz + 20%) is approximately 9 mV. This is optimistic when compared to the bench test results (since this SPICE simulation does not account for parasitics or cable termination imperfections). The intent of this simulation

is to demonstrate the potential for this fix and to provide confirmation for estimation of design margin.

Laboratory Test of the Solution #3:

Several bench tests were required to verify the proper functionality of this approach. It was discovered that subtle differences in cable length, cable termination, and driver configuration (e.g., on-enabled, on-disabled, powered-off) produced substantial variations in signal quality at the GARC receiver. After modifying the GSE board to be as flight-like as possible and using the most “flight-like” cables that we have, it was found that the source terminations were required. A sketch of the test setup is shown:

We used the two modified AEM simulator boards with the LabView software, using regtest6.vi to detect functional errors. We tested this solution at 3.0, 3.3, and 3.6V and at 20MHz and 24 MHz. We lowered the receiver terminating resistor to reduce the differential voltage at the receiver in order to measure the signal margin. Some of the results are listed in the table below.

Channel 1:	Brown,	ACD_CLK_P at receiver,	50 mV/div
Channel 2:	Blue,	ACD_CLK_M at receiver,	50 mV/div
Math1:	Ch1 – Ch2,	ACD clock differential,	50 mV/div
Channel 3:	Purple,	ACD_CLK_P at driver,	200 mV/div
Channel 4:	Green,	ACD_CLK_P at driver,	200 mV/div

In the table below, the ch1 – ch2 column represents the minimum switching voltage for pages 6 through 12. Pages 13 and 14 show the signals non-attenuated and with the proposed source and receiver terminations.

f (MHz)	V_{supply}	Scope Plot Taken	Scope M1 (ch1 – ch2)	Scope Bandwidth
20	3.0	see p. 6	33 mV	Full
20	3.3	see p. 7	33 mV	Full
20	3.6	see p. 8	43 mV	Full
24	3.0	see p. 9	44 mV	Full
24	3.3	see p. 10	44 mV	Full
24	3.6	see p. 11	48 mV	Full
24	3.6	see p. 12	40 mV	Limited
24	3.3	see p. 13	252 mV	Full
24	3.3	see p. 14	212 mV	Limited

All cases were similar (i.e., no dramatic voltage or frequency dependence). The worst case was shown at 24 MHz at a rail voltage of 3.6V. The minimum operating voltage measured in this case was a differential of 48 mV. The differential voltage with the proposed termination topology of three 100 ohm parallel resistors was measured at 252 mV. This provides for a measured worst-case room temperature design margin of $252/48 = 5.25$. Discussions with engineers here at Goddard confirm that a factor of 5 in signal margin is a reliable number to implement for a flight fix.

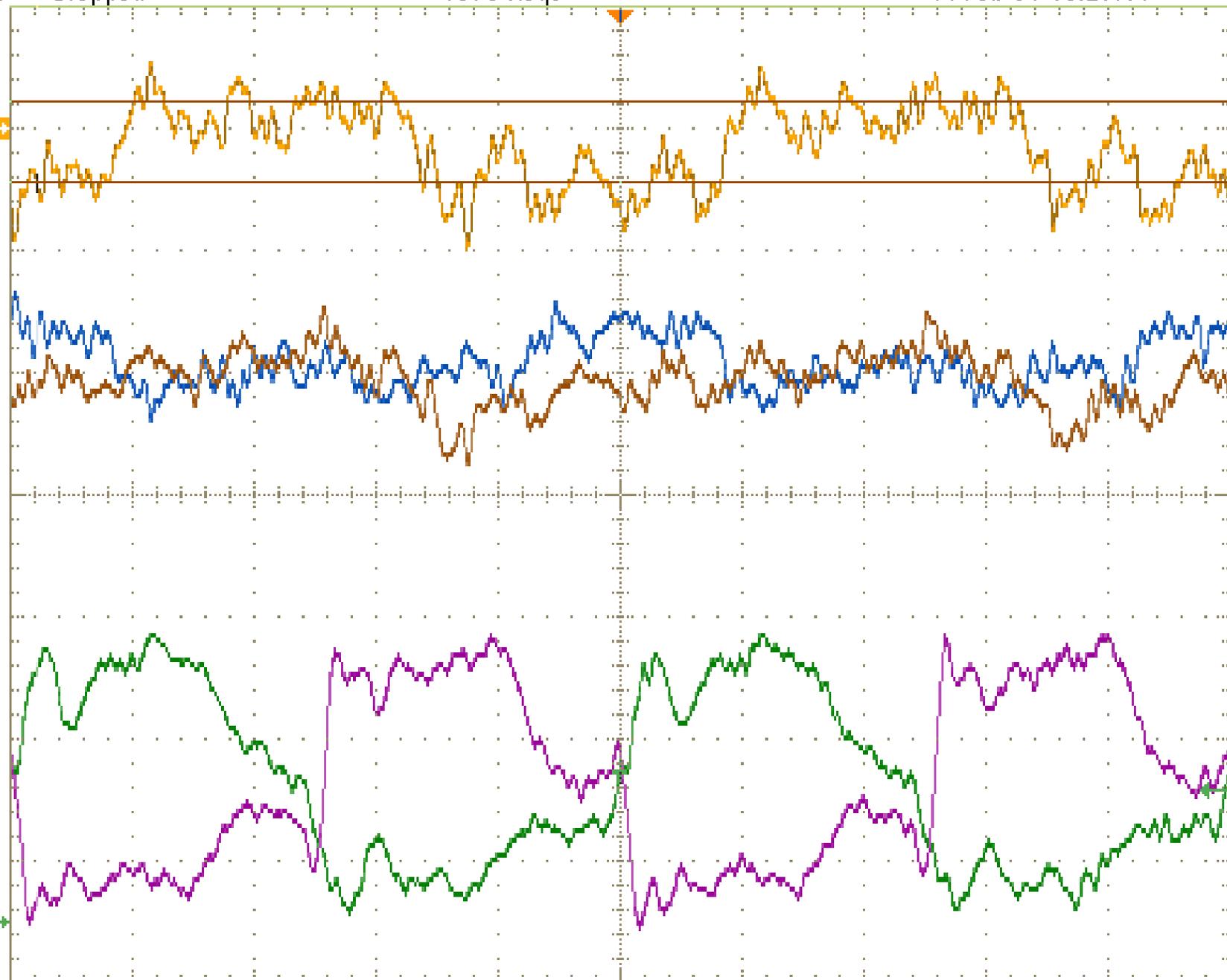
Tek Stopped

4876 Acqs

11 Feb 04 10:27:14

Buttons

VIC



Curs1 Pos
1.336V

Curs2 Pos
1.303V

V1 : 1.336V
V2 : 1.303V
 ΔV : -33.0mV

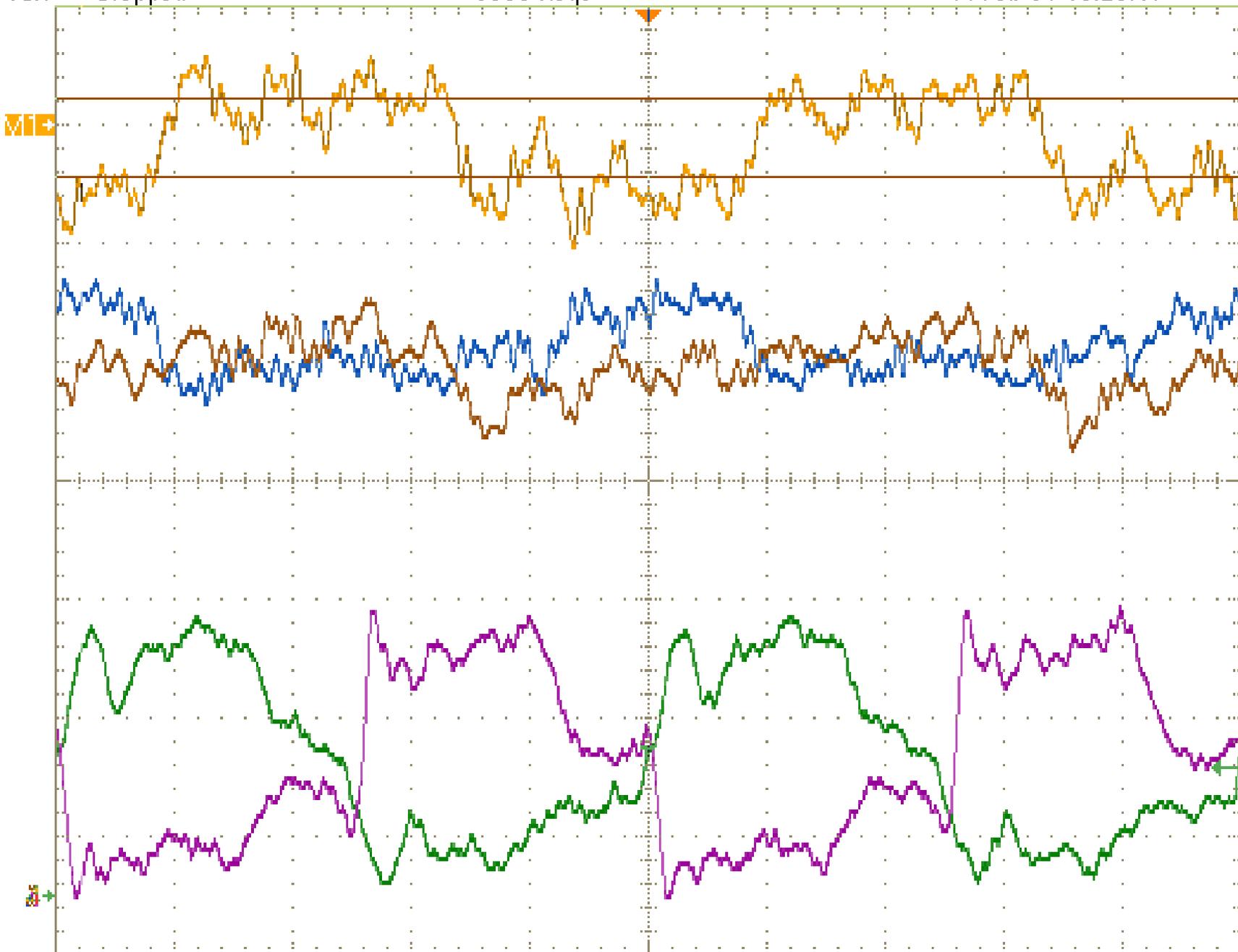
Ch1 50.0mV Ch2 50.0mV M 10.0ns 2.5GS/s IT 20.0ps/pt
Ch3 200mV Ch4 200mV A Ch4 \approx 1.22V
Math1 50.0mV 10.0ns

Tek Stopped

5930 Acqs

11 Feb 04 10:29:17

Buttons



Curs1 Pos
1.336V

Curs2 Pos
1.303V

V1 : 1.336V
V2 : 1.303V
 ΔV : -33.0mV

Ch1 50.0mV Ch2 50.0mV M 10.0ns 2.5GS/s IT 20.0ps/pt
Ch3 200mV Ch4 200mV A Ch4 1.22V
Math1 50.0mV 10.0ns

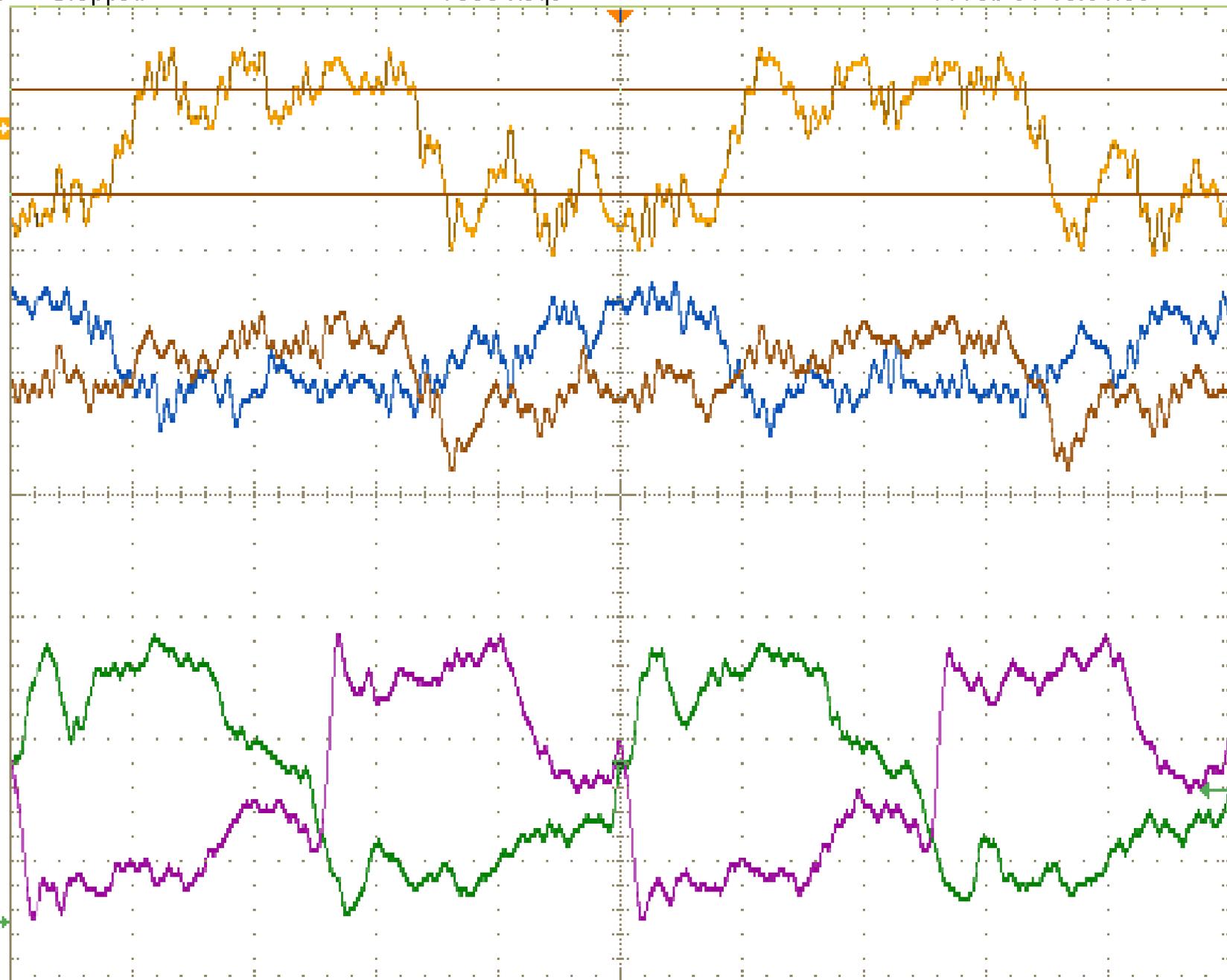
Tek Stopped

7566 Acqs

11 Feb 04 10:31:38

Buttons

VIC



Curs1 Pos
1.341V

Curs2 Pos
1.298V

V1 : 1.341V
V2 : 1.298V
 ΔV : -43.0mV

Ch1	50.0mV	Ch2	50.0mV	M	10.0ns	2.5GS/s	IT	20.0ps/pt
Ch3	200mV	Ch4	200mV	A	Ch4	1.22V		
Math1	50.0mV	10.0ns						

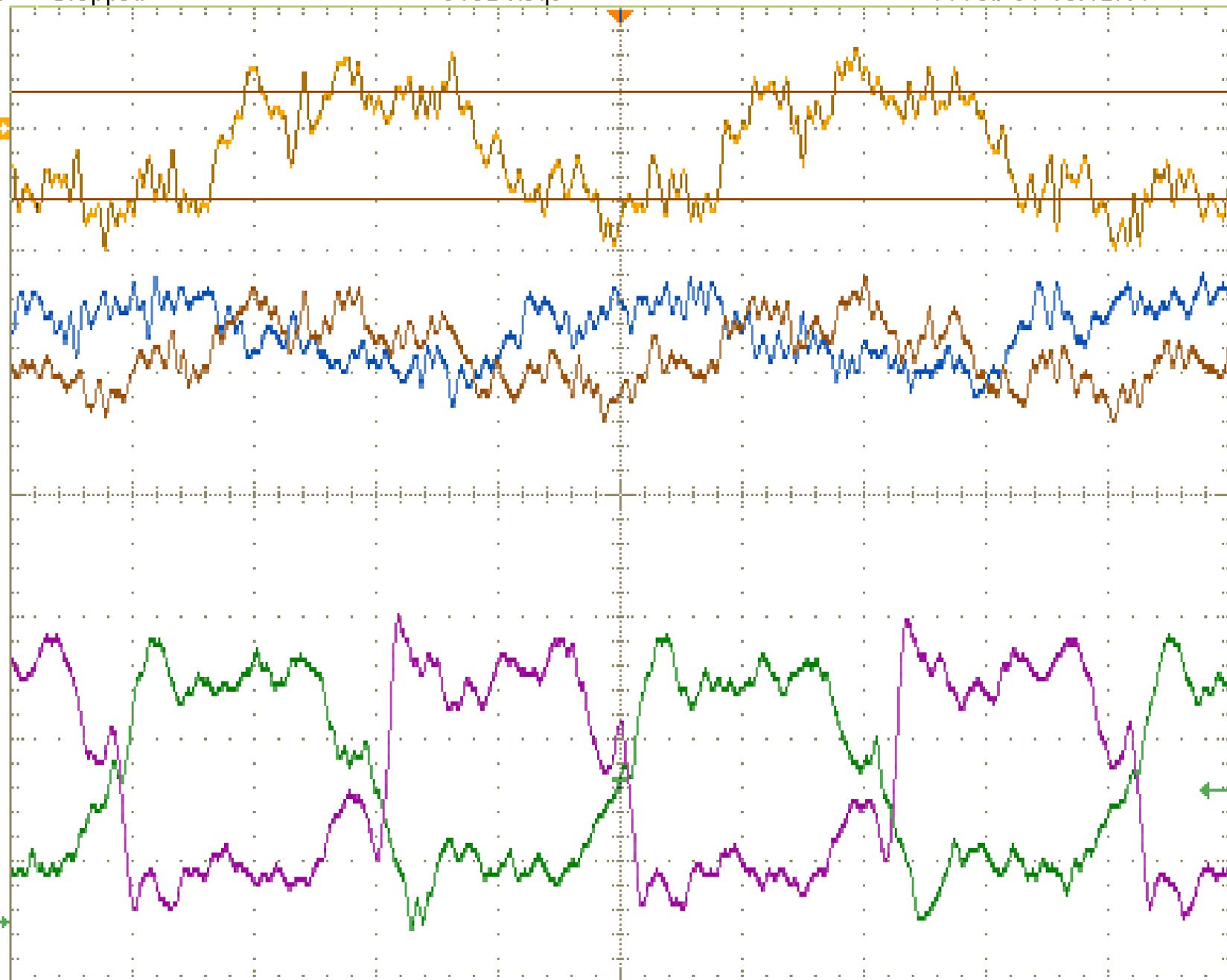
Tek Stopped

3432 Acqs

11 Feb 04 10:42:11

Buttons

VIC



Curs1 Pos

1.34V

Curs2 Pos

1.296V

V1 : 1.34V
V2 : 1.296V
 ΔV : -44.0mV

Ch1 50.0mV Ch2 50.0mV M 10.0ns 2.5GS/s IT 40.0ps/pt
Ch3 200mV Ch4 200mV A Ch4 1.22V
Math1 50.0mV 10.0ns

Tek Stopped

3905 Acqs

11 Feb 04 10:43:18

Buttons

V1

Curs1 Pos

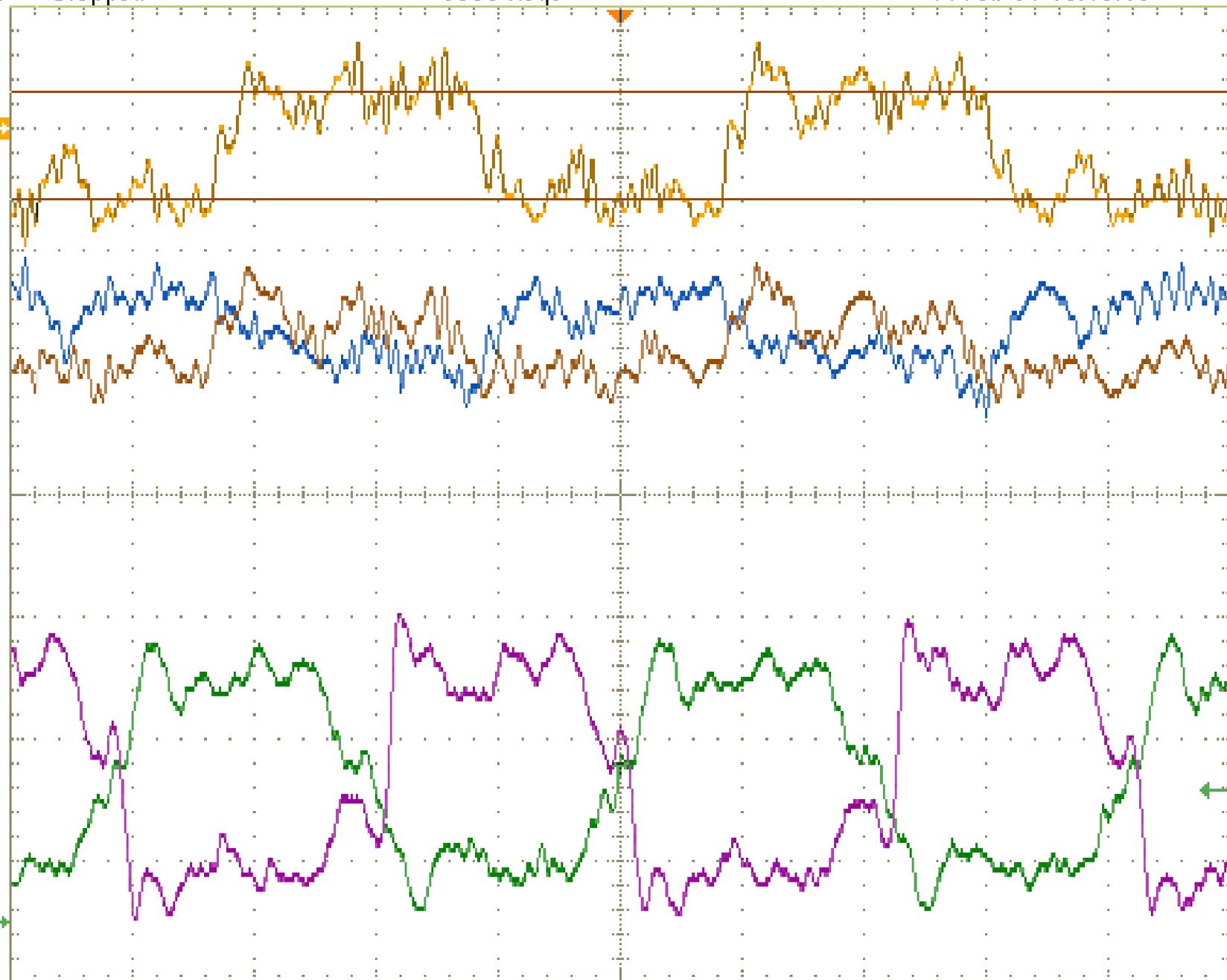
1.34V

Curs2 Pos

1.296V

V1 : 1.34V
V2 : 1.296V
 ΔV : -44.0mV

A



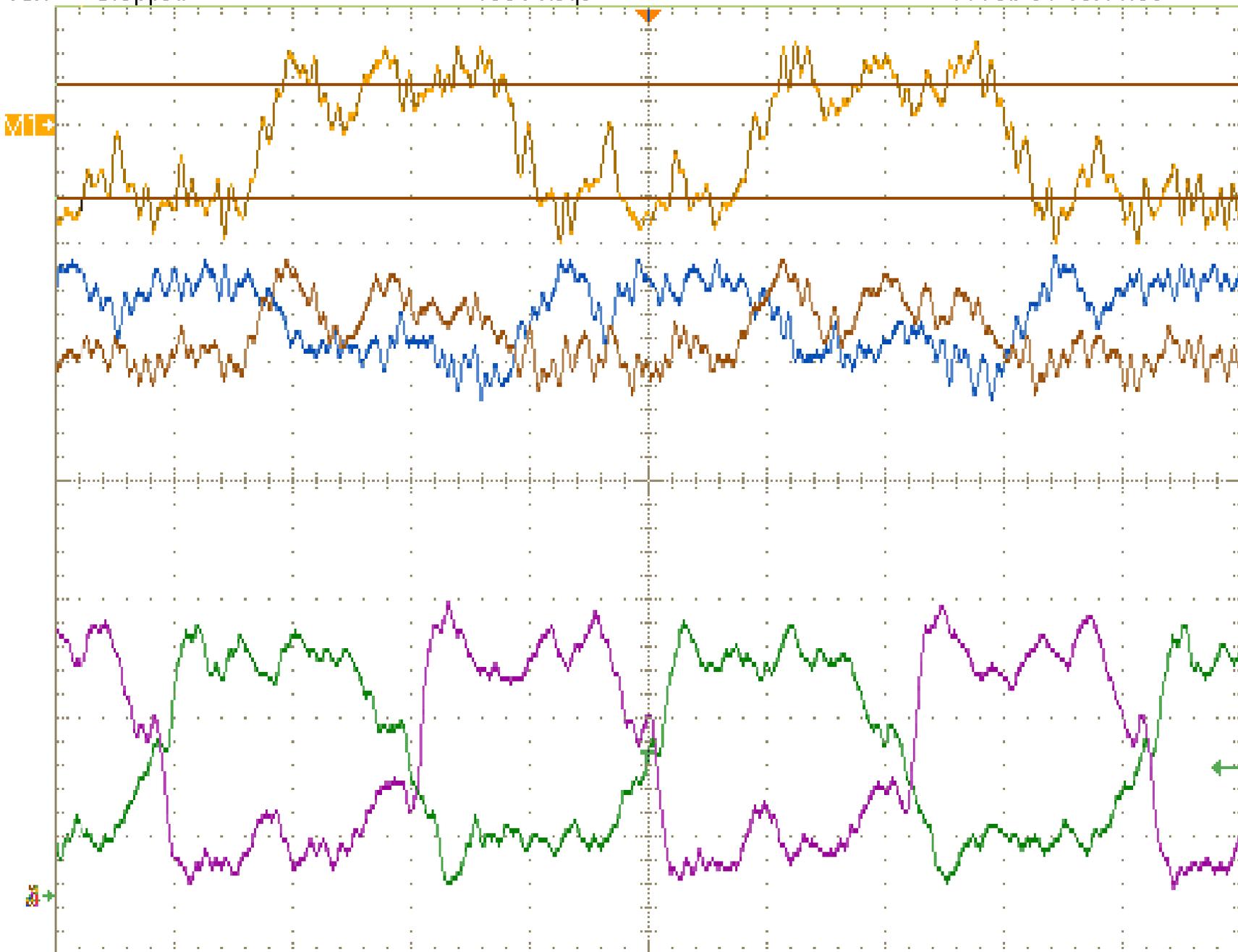
Ch1 50.0mV Ch2 50.0mV M 10.0ns 2.5GS/s IT 40.0ps/pt
Ch3 200mV Ch4 200mV A Ch4 \nearrow 1.22V
Math1 50.0mV 10.0ns

Tek Stopped

4834 Acqs

11 Feb 04 10:44:50

Buttons



Curs1 Pos
1.342V

Curs2 Pos
1.294V

V1 : 1.342V
V2 : 1.294V
 ΔV : -48.0mV

Ch1 50.0mV Ch2 50.0mV M 10.0ns 2.5GS/s IT 40.0ps/pt
Ch3 200mV Ch4 200mV A Ch4 1.22V
Math1 50.0mV 10.0ns

Tek Stopped

228 Acqs

11 Feb 04 10:46:09

Buttons

V1

Curs1 Pos

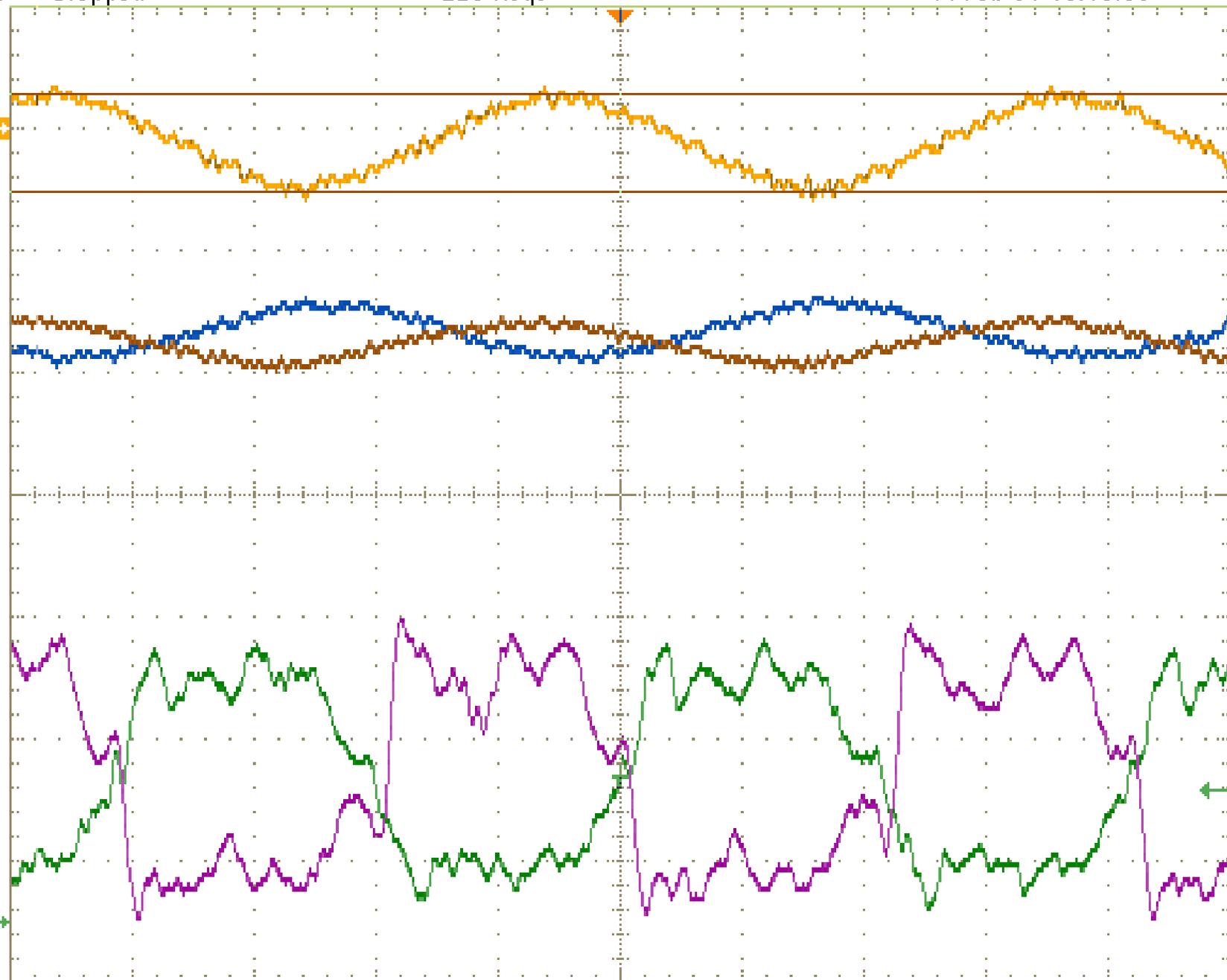
1.339V

Curs2 Pos

1.299V

V1 : 1.339V
V2 : 1.299V
ΔV : -40.0mV

ΔV



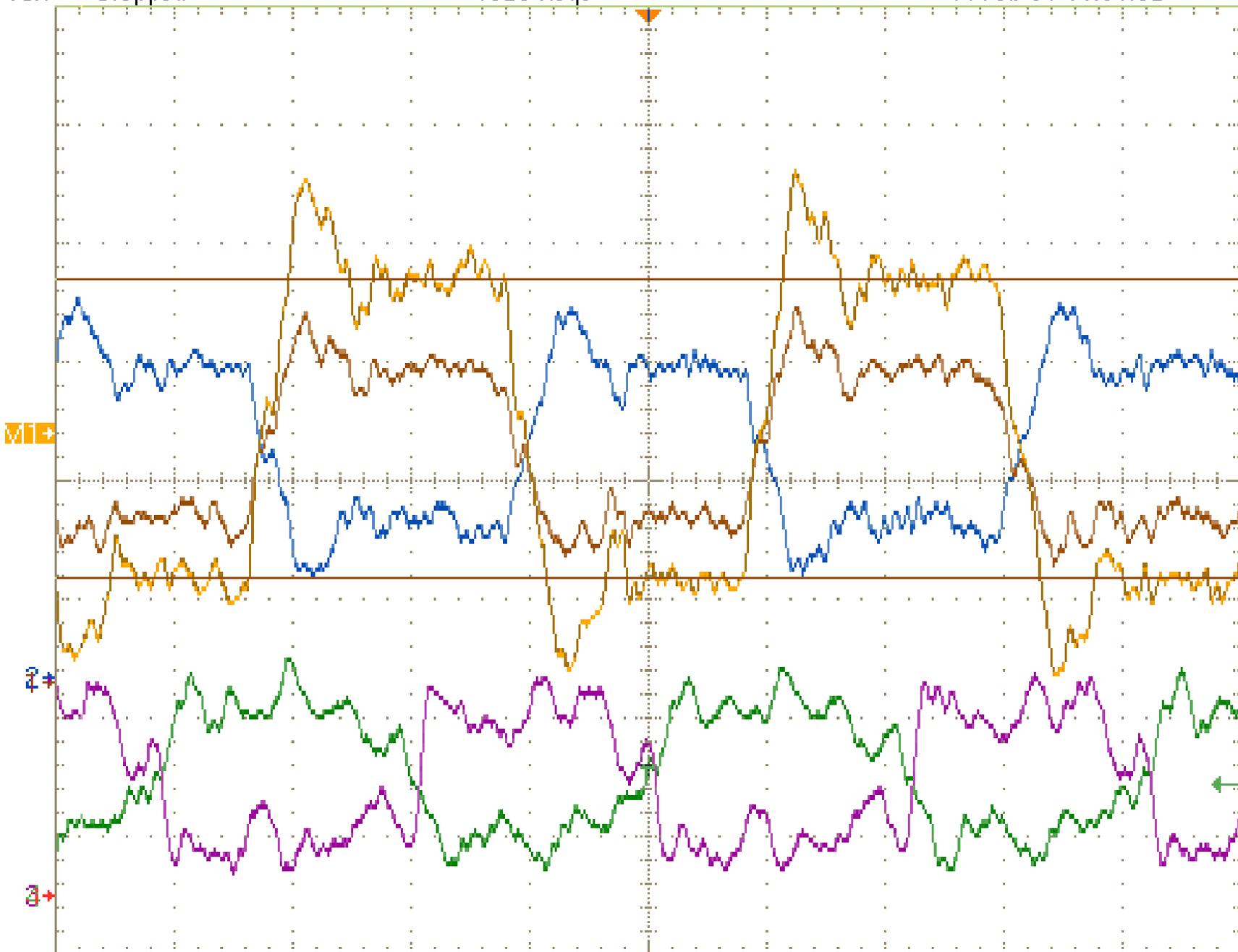
Ch1 50.0mV Bw Ch2 50.0mV Bw M 10.0ns 2.5GS/s IT 40.0ps/pt
 Ch3 200mV Ch4 200mV A Ch4 1.22V
 Math1 50.0mV 10.0ns

Tek Stopped

1526 Acqs

11 Feb 04 11:01:32

Buttons



Curs1 Pos

1.34V

Curs2 Pos

1.088V

V1 : 1.34V
 V2 : 1.088V
 ΔV : -252.0mV

V1 →

V2 →

→

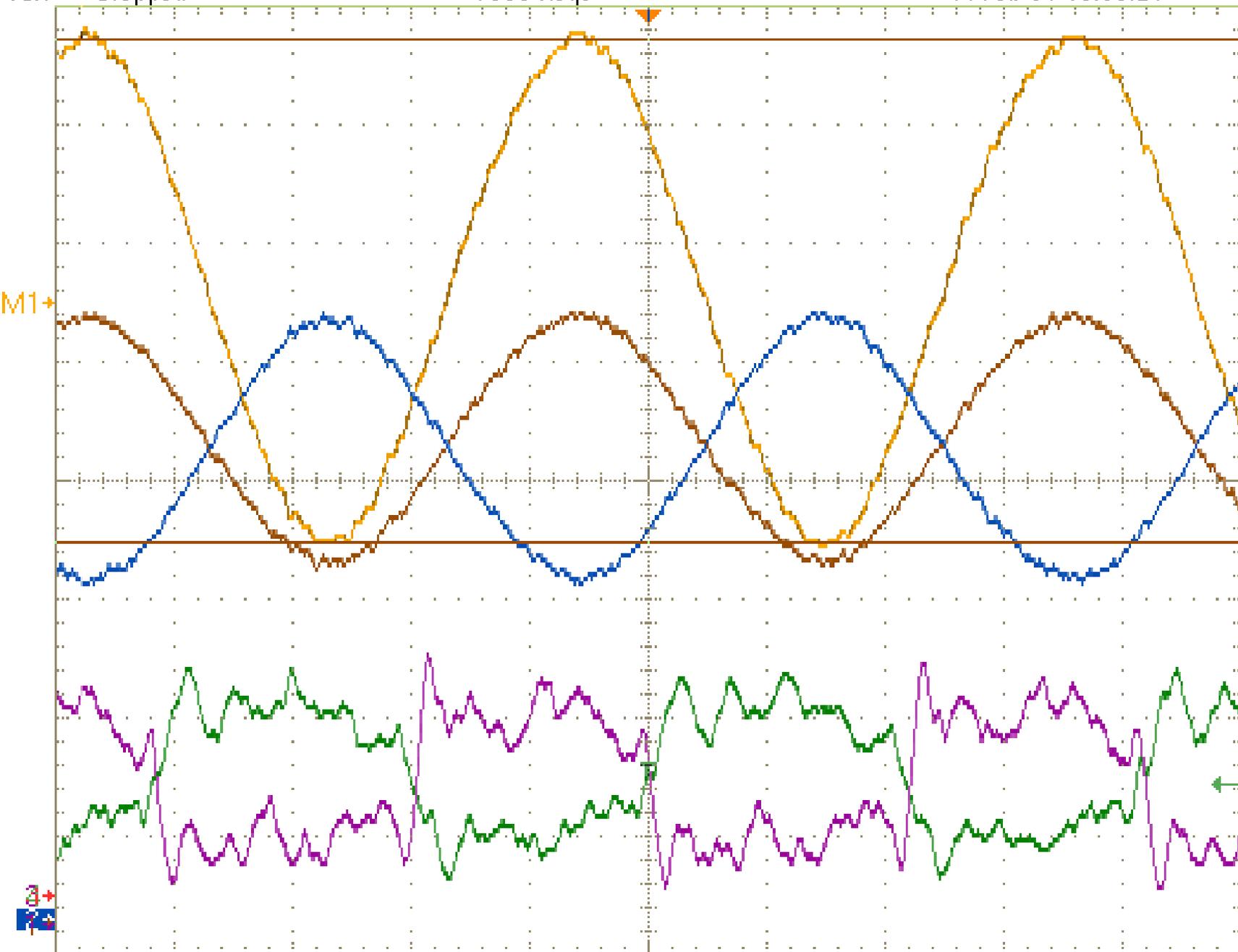
Ch1 100mV Ch2 100mV M 10.0ns 2.5GS/s IT 40.0ps/pt
 Ch3 200mV Ch4 200mV A Ch4 ✓ 1.19V
 Math1 100mV 10.0ns

Tek Stopped

7680 Acqs

11 Feb 04 10:55:24

Buttons



1.373V

1.161V

V1 : 1.373V
V2 : 1.161V
 ΔV : -212.0mV

Ch1 50.0mV Bw Ch2 50.0mV Bw M 10.0ns 2.5GS/s IT 40.0ps/pt
Ch3 200mV Ch4 200mV A Ch4 1.19V
Math1 50.0mV 10.0ns