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GAFE : GLAST ACD Front End Electronics ASIC

for

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Scope and Purpose:

This document describes the GAFE (GLAST ACD Front End Electronics) ASIC for the GLAST ACD (Anti Coincidence Detector). The documents briefly describes the requirements on the front end electronic ASIC and describes its architecture and its intended usage. This ASIC is presently being fabricated in Agilent/HP 0.5 um CMOS process.

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GLAST ACD Front End Electronics/ ASIC

1. Requirements / Specifications for GAFE ASIC:

.1 **Detector:** PMT, gain = 400,000
Anode_output (negative charge) to process signals in the range 0.1 MIP to 1000 MIPS

1.2 Charge Range: 0.1 MIP to 1000 MIPS
=> instrument dynamic range = 1 : 10,000
0.1 MIP <=> 1 Photo electron (pe) <=> 1.6 E-19 Coulombs
=> dynamic range = 1.6E-19 C to 1.6E-15 C

Since the gain of the PMT is 400,000, the charge input to the ASIC is as:
0.064PC for 0.1 MIP
0.64 PC for 1 MIP
640 PC for 1000 MIPS.

1.3 VETO generation: Generate a trigger output for signals above a nominal threshold of 0.3MIPs

1.3.1 VETO Threshold: Adjustable from 0.1 MIP to 2 MIP with a step size of 0.05 MIP or a charge range of 0.064pc to 1.28pc with a step size of 0.032PC

1.3.2 Veto Trigger Latency: latency for the entire ACD electronics chain within 600ns, the minimum latency expected is 150ns and is not likely to be less than 50ns. The jitter on the Veto trigger shall be less than or equal to 200 ns.

1.3.3 VETO Duration: longer than the time for baseline recovery to 0.05 MIP

1.3.4 Recovery to 1 MIP: For 1 MIP signal, VETO should be no longer than 1.2us

1.3.5 Recovery to Large Signals (1000 MIPS): VETO should be no longer than 10 us

1.3.6 VETO Signal Retrigger (Pulse Pile Up !): To be retriggerable within 50ns of the trailing edge.

(This should be handled by a VETO stretching Logic as described in the following text, this logic will be outside the ASIC)

1.4 CNO or HLD or High Level Threshold Detection: nominal threshold of 25 MIPS

1.4.1 CNO or HLD Threshold: Adjustable from 20 to 64 MIPS in steps of less than or equal to 1MIP

1.4.2 CNO or HLD Latency: latency no more than that of VETO signal.

1.5 LLD or ZS (Low Level Threshold or Zero Suppress) Signal: nominal threshold of 0.1 MIP

1.5.1 LLD or ZS Threshold: Adjustable from 0.05 MIP to 1 MIP in steps of 0.05 MIP

1.6 PHA (Pulse Height Analysis) output:

Low Energy / High Gain Channel:

Range: 0 to 10 Mips

Resolution: 0.1 MIP to 10 MIPs with a precision of 0.02 MIP or 5% which ever is larger

High Energy / Low Gain Channel:

Range: 0 to 1000 Mips

Resolution : for pulses above 20 MIPs and upto 1000 MIPs, a precision of 1 MIP or 2% which ever is larger

1.7 Test Charge Injection: ASIC to have mechanism for injecting test charge at the front end of electronics chain, the maximum injected charge will be 40pc (16pf * 2.5v), which corresponds to 62.5 MIPs.

1.8 Digitization: 10 or 12 bit ADC outside ASIC
5% Integral Non Linearity acceptable

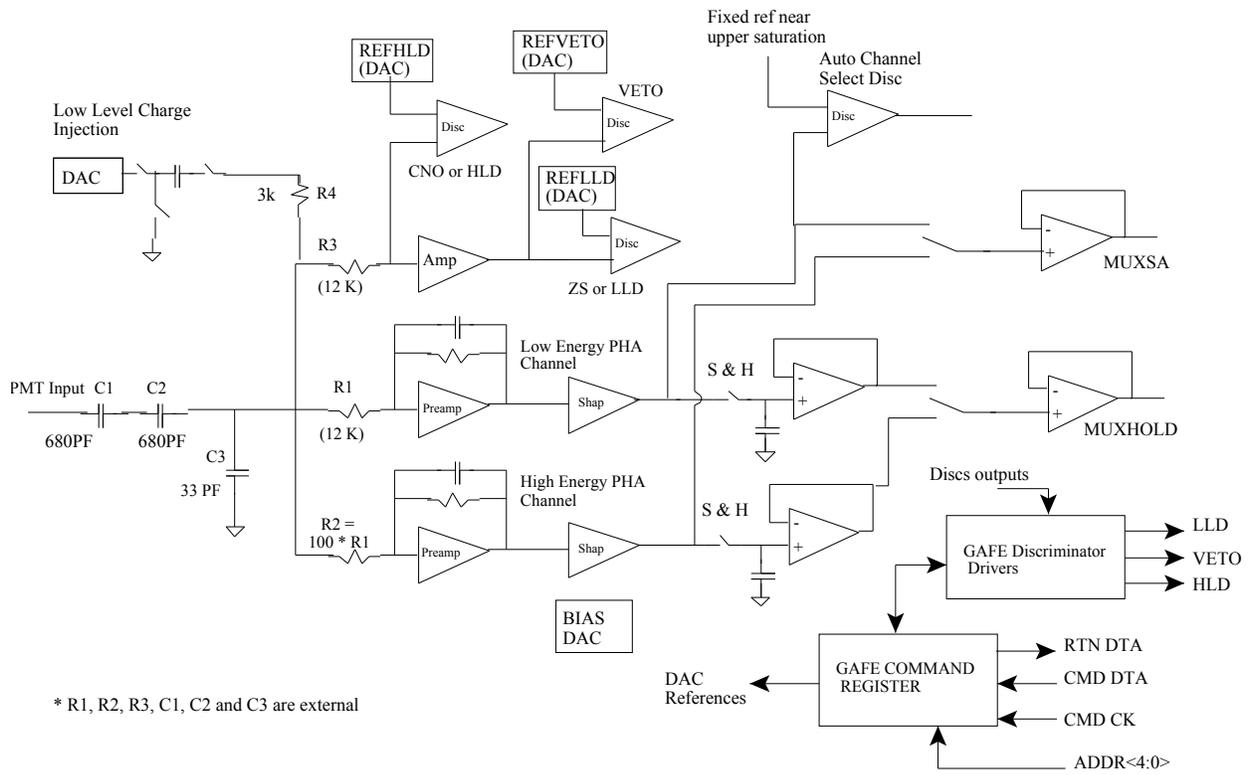
1.9 PMT Rise Time: for signal out of PMT : 3-5ns, 1ns for faster tubes

1.10 Event Rate: < 3 KHz per PMT
<= 5% of PMTs are expected to be digitized on an average

2. ASIC Architecture:

2.1 ACDFE1 1 : ASIC Overview:

The primary purpose of the ACD Front End Electronics ASIC is to receive the PMT signal, and process it after suitable amplification to generate fast triggers or discriminator outputs, and to



GLAST ACD Front End (GAFE) Analog ASIC : Conceptual Diagram

Fig. 1

shape and hold the signal for Pulse Height Analysis (PHA). The triggers that need to be generated are the VETO, the LLD or ZS, and the HLD or the CNO triggers.

In addition to the above analog circuits, this ASIC also contains the DACs to generate the various thresholds and biases, and also the digital modules which control the mode of operation of the chip and allow it to be interfaced to the outside electronics. The analog and digital subcircuits are described next. A simplified block schematic of the ASIC is given in Fig.1.

3. The Analog Front End

3.1 The Overview:

The analog front end comprises mostly of amplifiers and discriminators along with multiplexers, buffers and some other circuit modules. The main requirements that govern the front end electronics design are:

- (c) The dynamic range of 0.1 to 1000 MIP which for a PMT gain of 400,000 translates to 0.064 PC to 640 PC, this is a dynamic range of 1:10,000
- (c) Generation of a fast VETO trigger, preferably within 200ns for a 1 MIP signal
- (d) The desired peaking time for the PHA signal is 3us, a shorter time is not desirable as it will lead to greater errors due to timing jitter of the Sample Hold signal.

The various blocks of the analog circuit which are shown in Fig.1 are discussed next.

3.2 Amplifier with charge splitting:

The ACD requirements of 0.1MIP to 1000 MIPs dynamic range is too large to be handled by one channel of electronics with a fixed gain. To ease this requirement on electronics, it has been decided to split the electronics into two channels, a high gain channel going up to 10 MIPs, and a low gain channel going up to 1000 MIPs. In this approach two preamplifiers are used each with a series resistance at the input to the PMT, the charge that goes into each of the preamplifier is then inversely proportional to the resistance. This technique is used to handle a wide dynamic range such as required here.

In addition to the charge splitting resistances, an external cap of 33pf is used. The charge across this capacitor is bled by the two charge splitting resistances which are in series with two amplifiers which are also a part of slow shaping circuit required for PHA. The voltage signal developed across the capacitor is fed to the input of the discriminator through a series resistance. The charge splitting resistances and the capacitor are external to the ASIC.

3.3 Input Charge:

The design requirement calls for handling a signal range from 0.1 MIP to 1000 MIPs. A signal of 0.1 MIP generates 1 photo electron (pe) which has a charge of $1.6E-19$ C. Therefore, for a full scale input of 1000 MIPs, the charge generated is $1.6E-15$ C.

Since the gain of the PMT is 400,000, the charge input to the ASIC is, 0.064PC for 0.1 MIP, and 640 PC for 1000 MIPs.

For a charge collection capacitor of 33 Pf, the signal developed across it as required by the various discriminators is as:

0.1 MIP \Leftrightarrow 0.064 PC \Leftrightarrow 1.94 mv
1 MIP \Leftrightarrow 0.64 PC \Leftrightarrow 19.4 mv
10 MIPs \Leftrightarrow 6.4 PC \Leftrightarrow 194 mv
30 MIPs \Leftrightarrow 19.2 PC \Leftrightarrow 582 mv

50 MIPs \Leftrightarrow 32 PC \Leftrightarrow 970 mv

The choice of 33 Pf for the external charge collection capacitor therefore seems to be adequate as the voltage generated across it is within the input range of all the discriminators.

3.4 High Voltage Coupling Capacitors:

Since the charge is collected across a capacitor of 33 pf, the high voltage capacitors should be much larger than 33 pf. Since normally two capacitors are used in series, the use of two 680 Pf capacitors in series for high voltage decoupling is considered adequate.

3.5 Input time Constant / Discriminator Output duration:

The signal going into the input of the discriminator is an exponential pulse, the time constant of which is given by the product of input charge collection capacitor of 33 pf and the series resistance going into the low energy shaping amp.

Since the design requirements specify that the duration of the VETO signal be 1 us for 1 MIP signal, then the longest VETO duration would be obtained for the minimum threshold of 0.1 MIP and is given by the equation,

$$0.1 \text{ mip} = 1 \text{ mip} * \exp(-1 \text{ us}/\tau) \Rightarrow \tau = 0.43 \text{ us}$$

Therefore the time constant for signal going into the discriminators is chosen as 400 ns. This implies that the series resistance to the input of the low energy Shaping amp is given by,

$$r1 = 400 \text{ ns} / 33 \text{ pf} = 12 \text{ K}$$

Since the trailing edge of the VETO is stretched by 200 ns, the duration of VETO going out of ACD for 1 MIP is 1.2 us

3.6 Charge Splitting Resistors:

As discussed above, the input resistor to the High gain or the Low Energy channel is 12 K.

Since the High Energy channel has the full scale of 1000 MIPs which is 100 times the full scale of Low energy channel, the series resistance to the input of High energy channel is chosen as 100 times that of the resistance in the Low energy channel and is therefore equal to 1.2 MEG ohm.

3.7 Shaping Time for PHA:

The latency of the sample and hold from the LAT is 2us, therefore, the minimum peaking time of the shaped pulse is 2 us. However, since the resistor and caps fabricated in silicon can vary by 20% from one run to another, the peaking time should be increased to $2\text{us}/0.8/0.8 = 3.125 \text{ us}$. A peaking time of 3us has been chosen, this larger shaping time is of advantage as the error due to timing jitter in the Sample and Hold is smaller.

3.8 Fast Channel Amplification:

Since the signal range over which the VETO and Low Level (LLD) discriminators trigger is small, the signal across the input capacitor is first amplified by a gain of 20 before being fed to the VETO and LLD comparator circuits.

With reference to 3.3, the 0.1 MIP signal after amplification of 20 would now correspond to approx 40 mv which is large enough to satisfactorily trigger the comparator. The likely maximum signal of 2 MIP over which the VETO discriminator would be required to trigger would now correspond to approx 800 mv.

The input to the High Level (HLD) or CNO discriminator is not amplified as their the signal is already large enough.

3.9 Low Level Test Charge Injection:

An on chip capacitor of approximately 16 Pf has been fabricated, for a 2.5 v input, this would allow charge injection of 40 PC or 62.5MIPs. When not needed, the charge injection capacitor is disconnected by a switch that is activated by the Test Enable signal.

3.10 Zero Suppress (ZS) or Low Level Discriminator (LLD) : The threshold of this discriminator is set by signal labeled, “REFLLD”. Since the signal is negative going at the discriminator input and is at a base line of vdc1 (approx 1.5v), the reference is set to a level below vdc1. Therefore for zero level threshold setting, the reference should be set to vdc1 and for increasing signals, it should be decreased towards zero volts. The threshold setting is done by on chip DAC.

3.11 VETO Discriminator: The threshold of this discriminator is set by signal labeled, “REFVETO”. Since the signal is negative going at the discriminator input and is at a base line of vdc1 (approx 1.5v), the reference is set to a level below vdc1. Therefore for zero level threshold setting, the reference should be set to vdc1 and for increasing signals, it should be decreased towards zero volts. The threshold setting is done by on chip DAC.

3.12 CNO or High Level Discriminator (HLD) : The threshold of this discriminator is set by signal labeled, “REFHLD”. Since the signal at the discriminator input is at a base line of vdc1 (approx 1.5v), the reference is set to a level below vdc1. Therefore for zero level threshold setting, the reference should be set to vdc1 and for increasing signals, it should be decreased towards zero volts. The threshold setting is done by on chip DAC.

3.13 PMT Gain Drift: There is no gain adjustment on the ASIC. However, the gain of a group of PMTs is increased by increasing the high voltage so that the gain of the weakest PMT in that group is brought back up to the nominal level. To take care of the PMT gain variation from channel to channel, the threshold of the various discriminators for each channel or PMT are individually set by the on chip DACs.

A one time gain adjustment of the electronics chain is also possible by suitably selecting the external charge collection capacitor which is to be implemented on the board as a parallel combination of two capacitors.

3.14 Low Energy (LE) PHA Channel:

The low energy signal is amplified, shaped to peak at 3 μ s and feeds a sample hold circuit which is operated when a Hold signal is delivered from external to the chip.

3.15 High Energy (HE) PHA Channel:

The high energy channel is similar to the low energy channel. The signal is amplified, shaped to peak at 3 μ s and feeds a sample hold circuit which is operated when a Hold signal is delivered from external to the chip.

3.16 Sample and Hold:

The sample and hold comprises of a simple switch in series with the output of the final stage of shaping amplifier and a hold capacitor as shown in fig. 1. During normal operation, the switch is kept closed and the voltage across the hold capacitor tracks the output of the shaping amplifier, and when the hold signal is applied the signal across the capacitor is held.

3.17 Shaping Mux :

There is an on chip analog mux which selects the output of either the LE or HE shaping amp outputs. This mux is provided for testing of the circuits and is not required during flight.

3.18 Hold Mux:

There is an on chip analog mux which selects the output of either the LE or HE Sample and Hold outputs, the output of this mux is passed to the external ADC for digitization. The selection of the low or high energy channel can be performed in the Auto mode or the manual mode. In the auto mode, an on chip discriminator on the output of LE shaping amp senses if the signal is near the saturation and switches the mux to HE channel. In manual mode, the channel selection is under external control.

3.19 Auto Mode Channel Selection Comparator:

A discriminator is provided at the output of LE shaping amp and is set slightly below the upper saturation of the signal. When this discriminator fires, signaling a large signal, the Hold mux automatically switches to the HE channel when the ASIC is set to Auto mode.

3.20 Threshold settings:

On chip DACs are provided to set the various baselines and thresholds as needed by various sub circuits and discriminators. The DACs are described in the next section.

4. The DACs

4.1 The Overview:

The DACs are used to set the discriminator threshold as follows :

Signal	Min Setting	Max Setting	Step Size	No. of Bits
Veto	0 MIP	3.2 MIPs	0.05 MIP	6 bits
LLD	0 MIP	3.2 MIP	0.05 MIP	6 bits
HLD	0 MIP	64 MIPs	1 MIP	6 bits

Test Charge injection DAC, is also a 6 bit DAC that sets the voltage level to the test charge injection between 0 and 2.5 Volt.

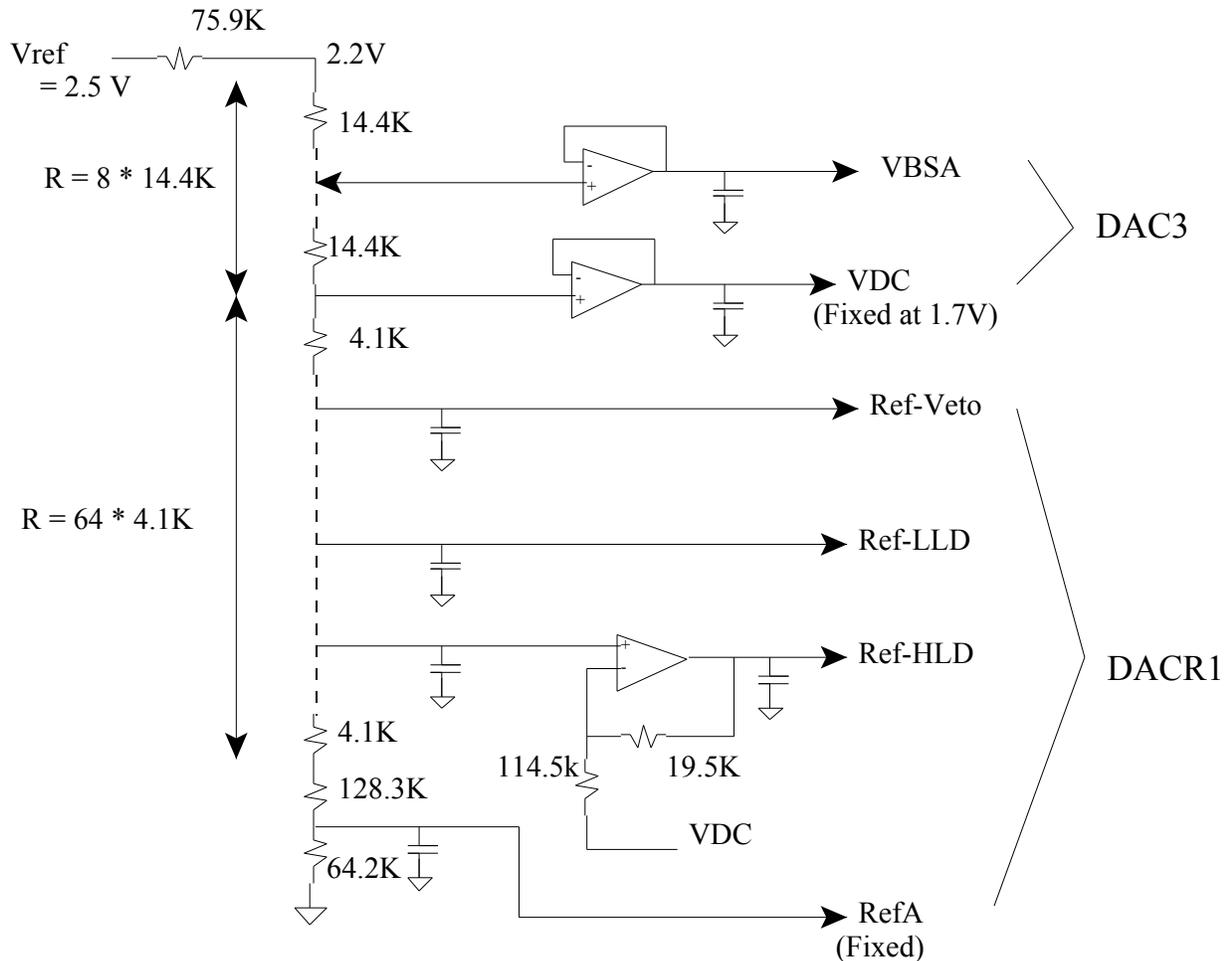
Base Line DAC is a 3 bit DAC that sets the baseline at the output of the Shaping Amps between 2.2 v and 1.75 v, the nominal setting is 2v.

The DAC block also generates fixed voltages for the following:

- Disc Base Line level: This is set to 1.75 v, the signal going into all the discriminators have a dc offset of this value of 1.75 v. The signal going into the discriminators is an inverted exponential in shape, and therefore the various thresholds are set below this baseline.
- Auto Channel Select Discriminator Level: This is set to 0.8V. When the signal in the low energy channel has exceeded the difference between this voltage and the DC base line at the shaping amp out, then the auto channel discriminator fires and this is used to switch the PHA to the high energy channel.

4.2 The DAC architecture:

The DACs are implemented using a resistive divider chain as shown in Fig.2. There are three DAC modules on the ASIC, DAC3 provides the level for the baseline at the output of the



An Overview of the DAC architecture in GAFE ASIC

Fig. 2:

Shaping amps and that at the input to the discriminators. DACR1 provides the threshold references for the discriminators. DACT provides the reference level for the on chip Test Charge injection circuit. As shown in Fig.2 , the DACs are formed using a resistive chain. DAC3 and DACR1 are in series with voltage reference which is set at 2.5 V. DACT is a separate chain of 64 resistors across Vref and ground, the output of this DAC determines the level of on chip Test charge injection. The structure and functioning of the various DACs is described next.

4.3 DAC3 : VBSA and VDC generation

The DAC3 is a 3 bit DAC that is formed by a series of 8 resistances each of 14.4K. This DAC is in series with a 75.9K resistor connected to the Vref which is set at 2.5V. The bottom end of the resistive chain is connected to the resistive chain for the 8 bit DACR1.

VBSA: The 3 bit DAC input is applied to a 3bit to 8 line decoder module that selects one of the 8 nodes in the resistive chain. The output of this resistive chain is buffered and made available as VBSA which is used to set the baseline at the output of shaping amps used for PHA. The nominal value of VBSA is 2v, this level can be set between 1.7V and 2.2V using the 3 bit DAC.

VDC: This voltage is fixed to 1.7V approximately and is made available from the bottom of the resistive chain comprising DAC3. This level determines the baseline at the input to the discriminators used to generate the various triggers.

4.4. DACR1: Threshold settings for Veto, LLD, HLD and PHA range select

This DAC comprises of 64 resistors in series. There are three 6 bit to 64 line decoders to independently select the threshold for each of the Veto, LLD and HLD. The level for PHA range select is fixed. Since this DAC is in series with DAC3 or the bottom node of DAC3 which determines the VDC level, the threshold settings are always guaranteed to be relative to the baseline (VDC) and therefore any drift in the baseline is not going to affect the performance of the discriminators.

Veto & LLD: Veto and LLD thresholds are set able in 64 steps with 6 bit DACs. Since these threshold are set to real low levels of the incoming signal, the signal from the PMT is first amplified by 20 before being fed to the Veto and LLD discriminators.

HLD: This sets the high level discriminator threshold., this is a 6 bit DAC which allows for 64 steps of settings.

Since the pulses are inverted, a signal of greater amplitude means setting the threshold farther below the baseline of VDC. The DAC setting of x3f or all "1"s, will set the threshold at the top or at VDC, which would actually mean a signal amplitude of zero. Conversely, a DAC setting of all "0"s would set the threshold at the bottom of the DAC which would correspond to full scale signal. Therefore the DAC bits should be set to x3f less the desired signal amplitude setting.

RefA: PHA range select threshold: This is a fixed voltage set near the full scale of the PHA. When the signal in the low energy channel PHA exceeds this threshold, the output of this discriminator is used to select the High energy channel for PHA. This level is presently set to 0.75 V.

4.5 DACT: Test Charge injection DAC

This DAC is also a 64 series resistor DAC strung across the Vref of 2.5 volts and ground. This 6 bit DAC determines the level of the test charge injection. An on chip capacitor of approximately 16 Pf has been fabricated, for a 2.5 v input, this would allow charge injection of 40 PC or 62.5MIPs.

5. The Digital Section

The GAFE ASIC contains a digital module that controls the various functions of the ASIC. The digital interface is through a serial data bus which comprises of a received data, return data and a clock. This serial link is implemented using low voltage differential signals, the chip is selected by an address ID for which there are 5 address pins available. The main function of the serial link is to program the various DACs, and set a few other parameters. The ASIC also outputs the various discriminator levels in a low voltage differential form, however to save on pins, the returns of some of the signals are tied together to form a common return. In addition, the digital module also selects the multiplexer channel to select either the high or low gain channel for PHA, controls the on chip test charge injection circuit, and operates the sample and hold.

The various digital signals will be described in the pinout section of this document.

6. The Pin Out

The various pins of the ASIC are described next. The ASIC has 48 bonding pads, the pin numbering starts from the top left and goes anticlockwise.

6.1 Supply Pins:

VCC: Pins: 1, 11: Analog Power, 3.3 V. These pins should have a 0.1 uf cap very close to the ASIC on the board the chip is mounted. If there is only enough space available for one 0.1 uf cap on the board, then it should be mounted close to pin 1.

Agnd: Pins: 2, 4, 6, 8, 12, 33, 35: Analog ground.

Vdd: Pins: 24, 38: Digital Power, 3.3V. These pins should have a 0.1 uf cap very close to the ASIC on the board the chip is mounted. If there is only enough space available for one 0.1 uf cap on the board, then it should be mounted close to pin 24

Dgnd: Pins: 13, 37,47. Digital ground.

6.2 Analog Pins:

salo: Pin 3: Slow Amp, Low Energy Input: This is the input for the low energy or high gain channel for the PHA. To this input, a 12K (R1) resistor is connected as shown in Fig.1. This resistor in conjunction with the R2 connected to sahi, splits the charge into two channels for PHA.

sahi: Pin 5: Slow Amp, High Energy Input: This is the input for the high energy or low gain channel for the PHA. To this input, a 1200K (R2) resistor is connected as shown in Fig.1. This resistor in conjunction with the R1 connected to salo, splits the charge into two channels for PHA.

discin: Pin 7: Input to the Fast channel for discriminators: To this a 12 K (R3) is connected as shown in Fig.1. This is a high impedance input to a fast shaping or large bandwidth amp. The output of this amp is to generate triggers for Veto and LLD.

Vref: Pin 9: 2.5 V Reference. This pin should be bypassed with a 0.1uf cap close to the ASIC. This is the reference input which is used by the DACs to generate the various discriminator thresholds and also is used to set the baseline for the shaping amps and of the signal that is input to the discriminators.

muxh: Pin 34: Multiplexer out for the Sampl and Hold outputs of the low and high energy PHA channels. This pin is connected to the ADC input.

muxsa: Pin 36: Multiplexer out for the shaping amp. This is the multiplexed shaping amp out for the low and high energy channels. This output is only meant for testing and diagnosis, it is not to be used on the final flight board.

tci: Pin 48: Test charge injection output. This is the charge injection output which is applied to the node where the two charge splitting resistances R1 and R2 meet, the connection to this node is via a 3k resistance is added as shown in Fig.1.

sparea: Pin 10: This is a spare pin associated with the analog modules.

6.3 The Digital Pns:

a0, a1, a2, a3, a4: Pns: 30, 31, 32, 44, 45 respectively: Address Pins: These pins are tied either to ground or to Vdd and determine the address or the ID of the ASIC.

LLD: Pin 29: This is the ZS or LLD out, this is a low voltage differential signal, but its return is in common with the Veto and Chnid. Having a common return, saves 2 pins per GAFE ASIC, and since there are 18 GAFE ASICs connected to one GARC ASIC, this results in a saving of 36 pins on the GARC.

VETO: Pin 28: This is the VETO out, this is a low voltage differential signal, but its return is in common with the LLD and Chnid. Having a common return, saves 2 pins per GAFE ASIC, and since there are 18 GAFE ASICs connected to one GARC ASIC, this results in a saving of 36 pins on the GARC.

chnid: Pin 27: A high indicates that high energy PHA channel has been selected for the multiplexed outputs. This is a low voltage differential signal, but its return is in common with the Veto and LLD. Having a common return, saves 2 pins per GAFE ASIC, and since there are 18 GAFE ASICs connected to one GARC ASIC, this results in a saving of 36 pins on the GARC.

irtn: Pin 26: This is the common return pin for signals LLD, VETO and chnid.

HLD2 and HLD1: Pins 18 and 19 respectively. This is a pseudo-differential out of the High level discriminator. Across these two pins is switch, which is turned on when the discriminator is fired, otherwise it is off. The HLDs from all the GAFE ASICs are tied together to implement an “OR” gate. When the HLD on any one of the 18 GAFE ASICs fires, the impedance between the HLD2 and HLD1 is lowered, and this is sensed by the GARC chip.

reset: Pin 25: This is the reset pin for digital logic.

Hold+ and Hold- : Pins 23 and 22 respectively: These are the differential hold inputs which make the PHA sample and hold circuit to switch from tracking to Hold mode

Strob+ and Strob- : Pins 21 and 20 respectively: These are differential strobe inputs, the signal which cause the charge injection of the on chip test pulser.

cmdd+ and cmdd- : Pins 41 and 42 respectively: These are low voltage differential inputs for the command data to the digital control module on the ASIC.

cmdck+ and cmdck- : Pins 39 and 40 respectively. These are low voltage differential inputs for the command clock to the digital control module on the ASIC.

rtnd: Pin 14: This is the return data from the digital block of GAFE ASIC.

state0, state1, state2: Pins 17, 16 and 15 respectively: These are the test outputs from the digital section of the GAFE ASIC and are meant for diagnosis only.

spared0 and spared1: Pins 43 and 46 respectively: These are spare pins associated with the digital modules of the GAFE ASIC.

7. Interfacing Issues:

7.1 Veto stretching:

The veto coming out of the ASIC should be stretched by 0.2us before it is passed on to the LAT, this allows 0.2us for the comparator to recover and be in a ready state to fire again if another signal arrived on the trailing edge of the stretched veto pulse. Assuming that the FPGA or the digital logic outside the ASIC can retrigger instantly after the trailing edge, the dead time of the ACD electronics is now effectively zero secs. However, since the electronics has finite rise, fall and delay times, there will be some finite time of dead time which will be unavoidable.

7.2 Hold Signal:

The latency of the sample and hold from the LAT is 2us, therefore, the minimum peaking time of the shaped pulse is 2 us. However, since the resistor and caps fabricated in silicon can vary by 20% from one run to another, the peaking time should be increased to $2\text{us}/0.8/0.8 = 3.125\text{ us}$. A peaking time of 3us has been chosen as the hold signal coming a little before the peak will not affect the linearity, but only reduce the gain slightly.

Therefore to sample the shaped signal at its peak value, the L1T trigger from the LAT should be delayed by 1us before sending it to the analog ACD ASIC. However, if the resistances and capacitors fabricated reveal that the actual value fabricated is 20% less than the designed, then the peaking time will occur at 2 us instead of 3us. For such cases the delay in the L1T trigger before it is applied as Hold signal to the analog ASIC should be zero. Conversely, if the resistance and capacitance values fabricated are 20% over, then the peaking will occur at 4.7 us. In this case, the L1T trigger should be delayed by $4.7 - 2 = 2.7\text{ us}$ before it is applied as a hold signal to the analog ASIC.

Thus there should be an adjustable delay in series with the Hold signal going into the analog ASIC, this delay should be adjustable from 0 to 2.7 us.