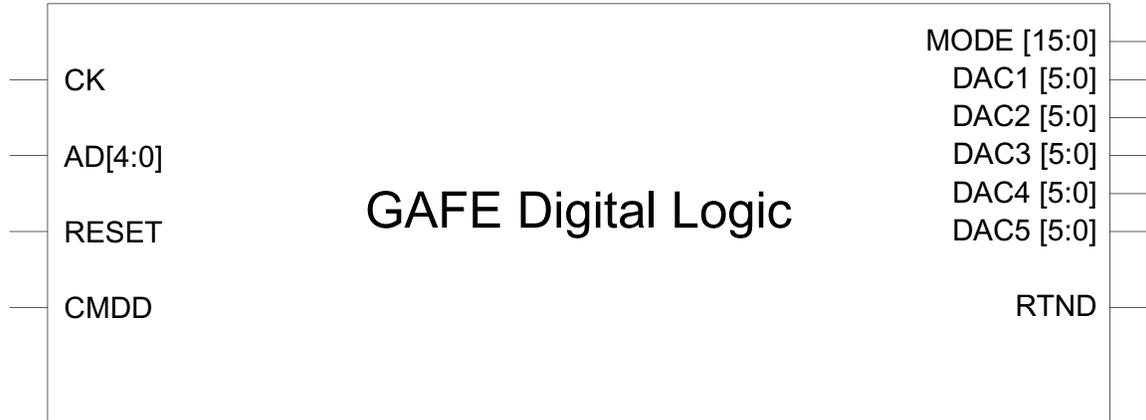


GAFE Timing & Interface Notes

(DRAFT, D. Sheppard, 1-18-02)

1.0 GAFE Logic Schematic / Documentation

The GAFE digital logic module is named *gafetop.v* and is represented by the following schematic symbol. The core logic module is wired to the pads (non-Tanner) in the GAFE by the analog designer.



Inputs to the module are the address bits (AD), the clock (CK), the configuration data (CMDD), and RESET. The output of the module transmitting data to the GARC is the return data, RTND. The register outputs are internal to the GAFE.

This module is written and simulated in Cadence Verilog-XL and synthesized with the Exemplar Leonardo toolset. Physical layout is accomplished via the Tanner tools. Documentation of the module consists of the following components:

1. Verilog behavioral code
2. Exemplar project database
3. Verilog structural (e.g., Tanner module specific) data files (EDIF and Verilog)
4. Tanner database
5. Physical layout extractions

Present versions being used are:

Cadence Verilog XL: 3.10.p001
Exemplar Leonardo: LeonardoSpectrum Level 3 - v2001_1b.12
Tanner L-Edit: 8.33

2.0 GAFE Logic Functionality

This module provides the following functions:

- Receives and processes configuration commands from the digital ASIC (GARC). These commands allow writing to one of the six registers.
- Receives and processes readback commands from the GARC. These commands allow readback of internal GAFE registers for configuration verification and diagnostic purposes.

The GAFE command format is as follows:

Bit 27	Start Bit	1
Bit 26	Read/Write Bit	Write = 0, Read = 1
Bits [25:21]	GAFE Address	Hardwired on FREE board
Bits [20:17]	GAFE Register Select	
Bits [16:1]	GAFE Command Data	
Bit 0	Parity Bit	Parity is Odd

Some time is required between commands. In the case of configuration commands, there should be 8 trailing zero bits sent. In the case of readback commands, there should be 28 trailing zero bits sent.

The GAFE return data back to the GARC is of the following format:

Bit 16	Start Bit	1
Bits [15:0]	GAFE Readback Data	

This data is sent to the GARC with an inverted polarity on RTND (e.g., start bit = GND) to allow for a wire-OR pullup for all 18 GAFEs on the FREE circuit card.

The positive edge of the CK is used for all logic. RESET is asynchronously asserted and synchronously deasserted.

The mode register is 16 bits. For the DAC registers, which are 6 bits, the GAFE return data most significant bits are padded with zeroes.

3.0 GAFE Register Assignments

The GAFE register contents and addresses are as follows:

Register 0:

mode[15:0]: GAFE "MODE" control register

bit [0]	:	TCI Gain:	0 = lo	, 1 = hi	, default = 0
bit [1]	:	TCI Pulse Enable:	0 = disable	, 1 = enable	, default = 1
bit [2]	:	Autorange select:	0 = manual	, 1 = auto	, default = 1
bit [3]	:	SA select bit:	0 = lo range	, 1 = hi range	, default = 0
bit [4]	:	VETO disc enable,	0 = disable	, 1 = enable	, default = 1
bit [5]	:	HLD disc enable,	0 = disable	, 1 = enable	, default = 1
bits [11: 6]	:	Spare mode bits			default = 0
bits [15:12]	:	Hardware version ID bits			

Note that the Hardware version ID bits are not commandable, but fixed. The Spare mode bits are commandable and may be used by the analog designer for any functions that are required.

Register 1: "VETO" DAC1 [5:0]: DAC #1 control register. Power up default = 5'h1F.

Register 2: "HLD" DAC2 [5:0]: DAC #2 control register. Power up default = 5'h1F.

Register 3: "TCI" DAC3 [5:0]: DAC #3 control register. Power up default = 5'h1F.

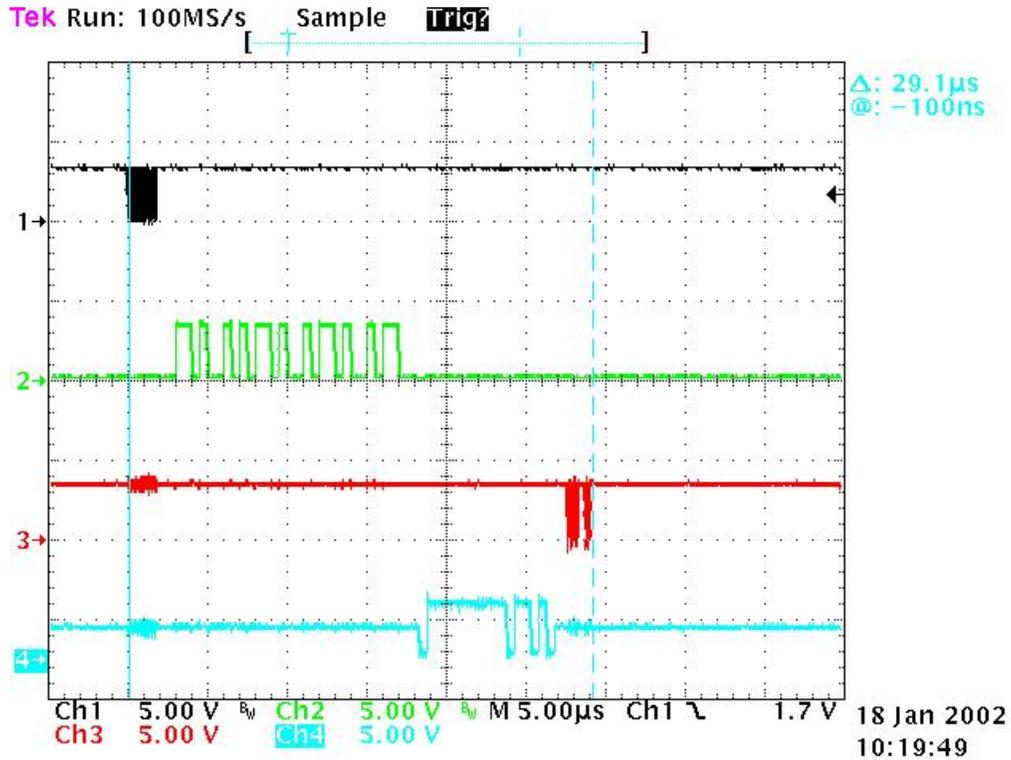
Register 4: "BIAS" DAC4 [5:0]: DAC #4 control register. Power up default = 5'h1F.

Register 5: DAC5 [5:0]: DAC #5 control register. Power up default = 5'h1F. Note that these DAC control bits are presently unused in the design, but are available for future use.

Commands to non-existent register addresses are processed with no change in state of the GAFE registers.

4.0 GAFE Logic Timing Measurements

The GAFE logic has been implemented at the following timing relationships have been captured on the oscilloscope. The GARC clock used was the nominal 20 MHz. The GAFE clock used was 2 MHz (the present spec on the design from the analog designer).



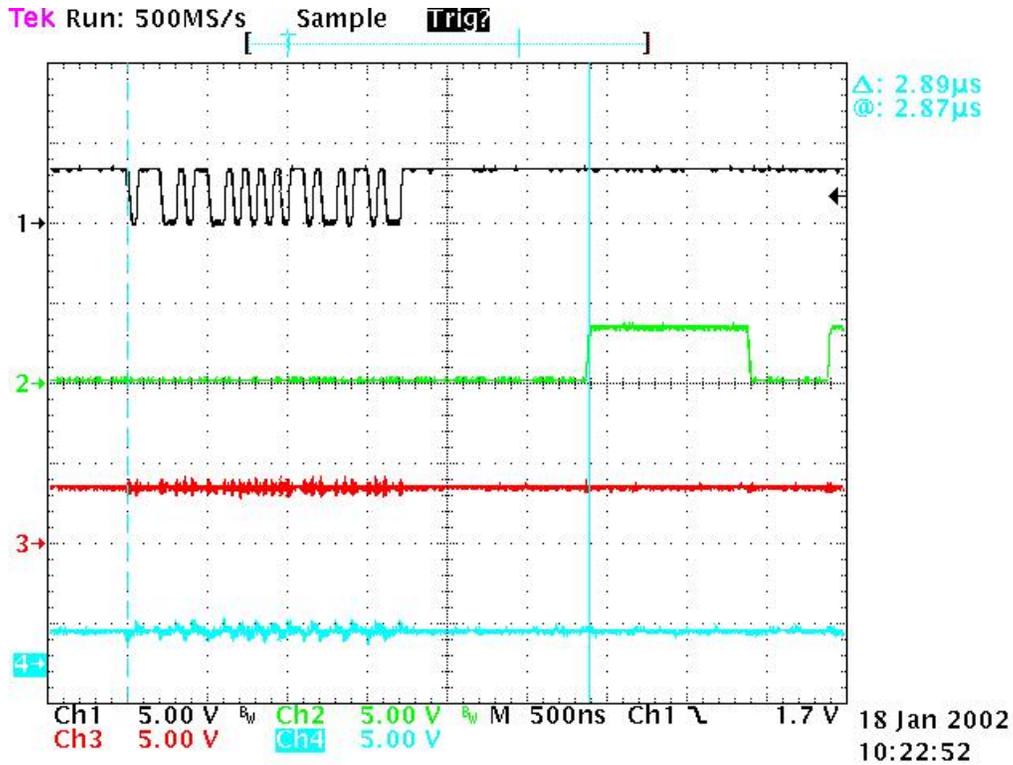
Trace #1 shows the AEM to GARC command

Trace #2 shows the GAFE command data from the GARC

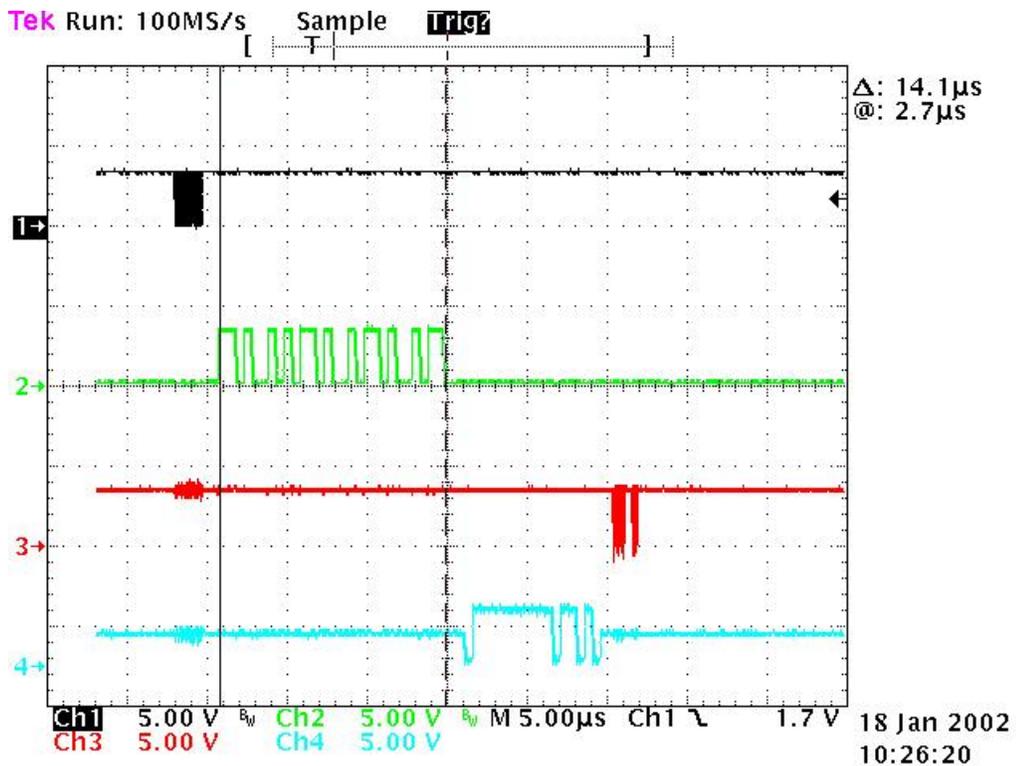
Trace #4 shows the GAFE readback data to the GARC

Trace #3 shows the GARC readback data to the AEM

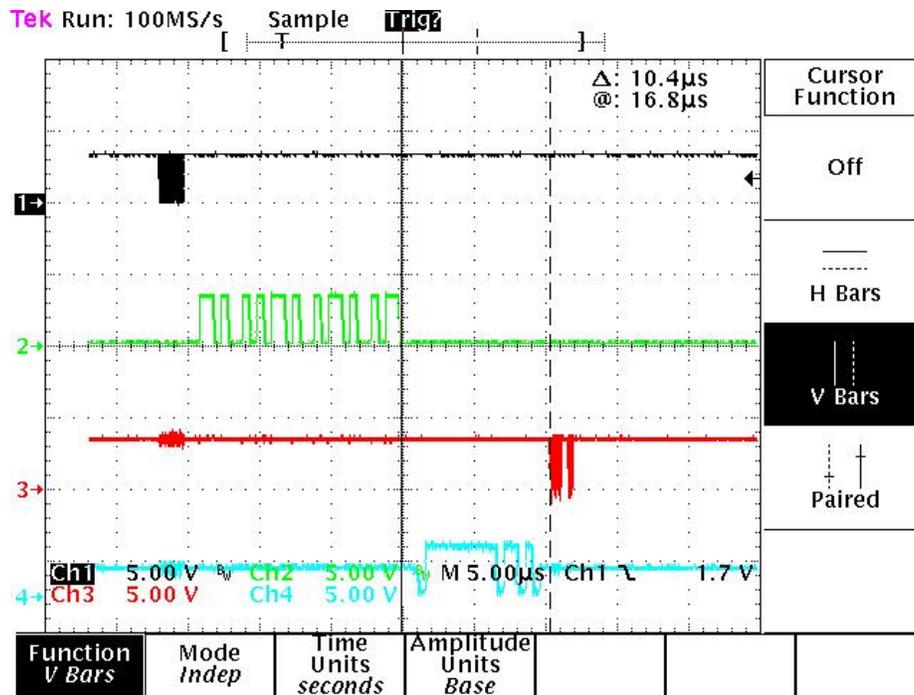
At 2 MHz, the entire sequence takes approximately 29.1 μsec.



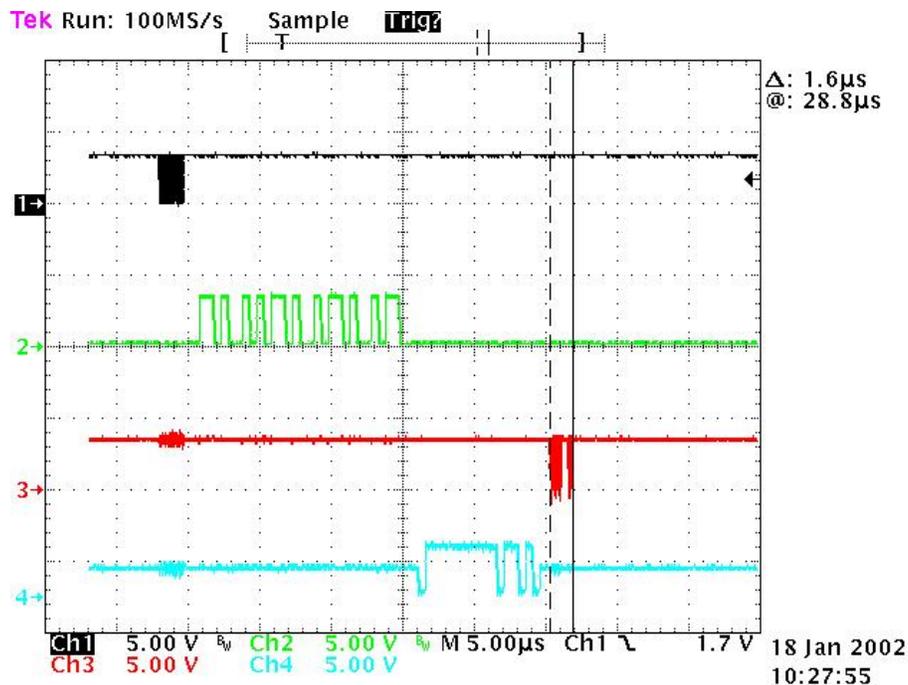
As shown above, the time to receive and process the command from the AEM in the GARC is measured at 2.9 μsec from GARC start bit to GAFE start bit.



The time of the GAFE command execution is measured to be 14.1 μ sec at 2 MHz. If the clock frequency were raised to 5 MHz, this time could be decreased to approximately 5.7 μ sec.

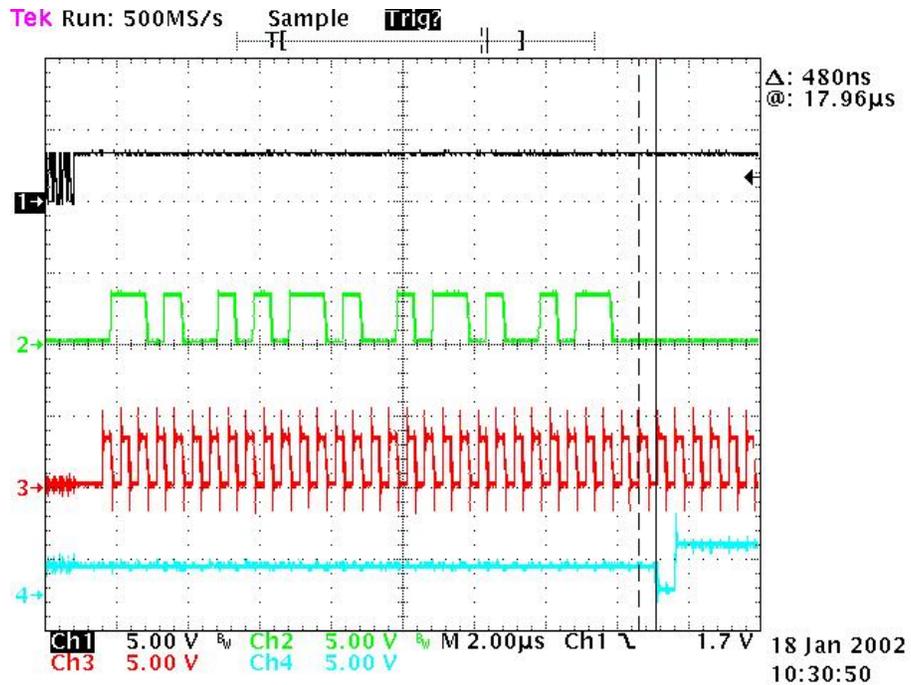


The time of the GAFE readback execution is measured at 10.4 μ sec at 2 MHz. If the clock frequency were increased to 5 MHz, this time would be reduced to approximately 4.2 μ sec.



The readback of the GAFE configuration to the AEM via GARC return data is measured at 1.6 μ sec.

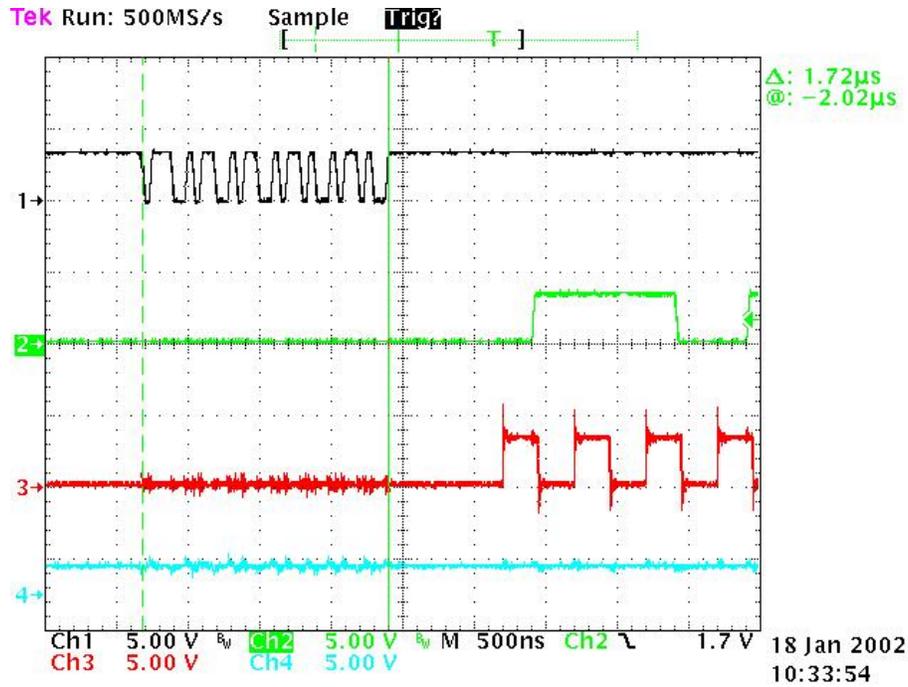
The total execution time at 2 MHz is measured at $2.9 + 14.1 + 10.4 + 1.6 = 29$ μ sec. If the CK frequency were increased to 5 MHz, this time would be reduced to $2.9 + 5.7 + 4.2 + 1.6 = 14.4$ μ sec.



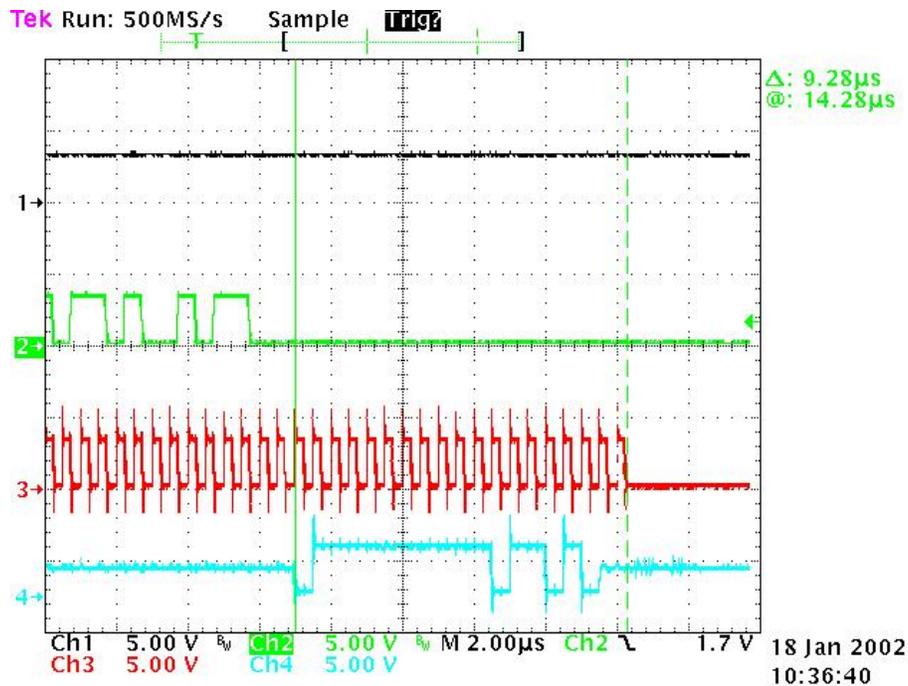
Timing of the GAFE clock and data

Channel 2 is the GAFE CMDD

Channel 3 is the GAFE CK.



**Timing Relationship between
 GARC command, GAFE CMDD, and GAFE CK**



**Timing Relationship between
 end of GAFE command, GAFE readback data
 and GAFE clock**