	A	B	C	D	F	G	H	I	K
1	**5/13/2002**	**GARC Version 1**							
2	Signal Description	Tanner	MOSIS Bond Pad Name	GARC	In (I)	PAD SIGNAL NAME	CORE SIGNAL NAME	TRUE	Tanner Block I/O
3		I/O		Pad	Out (O)				
4		Cell		No.	Pow (P)				
5					Bias (B)				
6					Iret (R)				
7									
8	Digital Ground	PADGnd	L1	1	P	DGND			
9	Clock+ to ACD from AEM A	PADAREF	L2	2	I	ACD_CLK_AP	ACD_CLK_A	H	RCVRF With no R between P and M,150uA preset I
10	Clock- to ACD from AEM A	PADAREF	L3	3	I	ACD_CLK_AM			Need Termination Resistor on the Board
11	Clock+ to ACD from AEM B	PADAREF	L4	4	I	ACD_CLK_BP	ACD_CLK_B	H	RCVRF With no R between P and M,150uA preset I
12	Clock- to ACD from AEM B	PADAREF	L5	5	I	ACD_CLK_BM			Need Termination Resistor on the Board
13	Command+ to ACD from AEM A	PADAREF	L6	6	I	ACD_NSCMD_AP	ACD_NSCMD_A	L	RCVRF With no R between P and M,150uA preset I
14	Command- to ACD from AEM A	PADAREF	L7	7	I	ACD_NSCMD_AM			Need Termination Resistor on the Board
15	Command+ to ACD from AEM B	PADAREF	K8	8	I	ACD_NSCMD_BP	ACD_NSCMD_B	L	RCVRF With no R between P and M,150uA preset I
16	Command- to ACD from AEM B	PADAREF	L9	9	I	ACD_NSCMD_BM			Need Termination Resistor on the Board
17	Reset+ to ACD from AEM A	PADAREF	L10	10	I	ACD_NRST_AP	ACD_NRESET_A	L	RCVRF With no R between P and M,150uA preset I
18	Reset- to ACD from AEM A	PADAREF	L11	11	I	ACD_NRST_AM			Need Termination Resistor on the Board

	A	B	C	D	F	G	H	I	K
19	Reset+ to ACD from AEM B	PADAREF	L12	12	I	ACD_NRST_BP	ACD_NRESET_B	L	RCVRF With no R between P and M,150uA preset I
20	Reset- to ACD from AEM B	PADAREF	L13	13	I	ACD_NRST_BM			Need Termination Resistor on the Board
21	Data+ to AEM A	PADAREF	L14	14	O	ACD_NSDATA_AP	ACD_NSDATA	L	LLDRV7, 3.5mA Max.LVDS Driver
22	Data- to AEM A	PADAREF	L15	15	O	ACD_NSDATA_AM			
23	Data+ to AEM B	PADAREF	L16	16	O	ACD_NSDATA_BP	ACD_NSDATA	L	LLDRV7, 3.5mA Max.LVDS Driver
24	Data- to AEM B	PADAREF	L17	17	O	ACD_NSDATA_BM			
25	CNO + to AEM A	PADAREF	L18	18	O	ACD_NCNO_AP	ACD_NCNO	L	LLDRV7, 3.5mA Max.LVDS Driver
26	CNO - to AEM A	PADAREF	L19	19	O	ACD_NCNO_AM			
27	CNO + to AEM B	PADAREF	L20	20	O	ACD_NCNO_BP	ACD_NCNO	L	LLDRV7, 3.5mA Max.LVDS Driver
28	CNO - to AEM B	PADAREF	L21	21	O	ACD_NCNO_BM			
29	Veto Ch 0 + to AEM A	PADAREF	L22	22	O	ACD_NVETO_00AP	ACD_NVETO_00	L	LLDRV7, 3.5mA Max.LVDS Driver
30	Veto Ch 0 - to AEM A	PADAREF	L23	23	O	ACD_NVETO_00AM			
31	Digital Power	PADVdd	L24	24	P	DVDD			
32	Veto Ch 0 + to AEM B	PADAREF	L25	25	O	ACD_NVETO_00BP	ACD_NVETO_00	L	LLDRV7, 3.5mA Max.LVDS Driver
33	Veto Ch 0 - to AEM B	PADAREF	L26	26	O	ACD_NVETO_00BM			
34	Digital Ground	PADGnd	L27	27	P	DGND			
35	Veto Ch 1 + to AEM A	PADAREF	L28	28	O	ACD_NVETO_01AP	ACD_NVETO_01	L	LLDRV7, 3.5mA Max.LVDS Driver
36	Veto Ch 1 - to AEM A	PADAREF	L29	29	O	ACD_NVETO_01AM			
37	Veto Ch 1 + to AEM B	PADAREF	L30	30	O	ACD_NVETO_01BP	ACD_NVETO_01	L	LLDRV7, 3.5mA Max.LVDS Driver
38	Veto Ch 1 - to AEM B	PADAREF	L31	31	O	ACD_NVETO_01BM			
39	Veto Ch 2 + to AEM A	PADAREF	L32	32	O	ACD_NVETO_02AP	ACD_NVETO_02	L	LLDRV7, 3.5mA Max.LVDS Driver

	A	B	C	D	F	G	H	I	K
40	Veto Ch 2 - to AEM A	PADAREF	L33	33	O	ACD_NVETO_02AM			
41	Veto Ch 2 + to AEM B	PADAREF	L34	34	O	ACD_NVETO_02BP	ACD_NVETO_02	L	LLDRV7, 3.5mA Max.LVDS Driver
42	Veto Ch 2 - to AEM B	PADAREF	L35	35	O	ACD_NVETO_02BM			
43	Veto Ch 3 + to AEM A	PADAREF	L36	36	O	ACD_NVETO_03AP	ACD_NVETO_03	L	LLDRV7, 3.5mA Max.LVDS Driver
44	Veto Ch 3 - to AEM A	PADAREF	L37	37	O	ACD_NVETO_03AM			
45	Veto Ch 3 + to AEM B	PADAREF	L38	38	O	ACD_NVETO_03BP	ACD_NVETO_03	L	LLDRV7, 3.5mA Max.LVDS Driver
46	Veto Ch 3 - to AEM B	PADAREF	L39	39	O	ACD_NVETO_03BM			
47	Veto Ch 4 + to AEM A	PADAREF	L40	40	O	ACD_NVETO_04AP	ACD_NVETO_04	L	LLDRV7, 3.5mA Max.LVDS Driver
48	Veto Ch 4 - to AEM A	PADAREF	L41	41	O	ACD_NVETO_04AM			
49	Veto Ch 4 + to AEM B	PADAREF	L42	42	O	ACD_NVETO_04BP	ACD_NVETO_04	L	LLDRV7, 3.5mA Max.LVDS Driver
50	Veto Ch 4 - to AEM B	PADAREF	L43	43	O	ACD_NVETO_04BM			
51	Veto Ch 5 + to AEM A	PADAREF	L44	44	O	ACD_NVETO_05AP	ACD_NVETO_05	L	LLDRV7, 3.5mA Max.LVDS Driver
52	Veto Ch 5 – to AEM A	PADAREF	L45	45	O	ACD_NVETO_05AM			
53	Veto Ch 5 + to AEM B	PADAREF	L46	46	O	ACD_NVETO_05BP	ACD_NVETO_05	L	LLDRV7, 3.5mA Max.LVDS Driver
54	Veto Ch 5 – to AEM B	PADAREF	L47	47	O	ACD_NVETO_05BM			
55	Veto Ch 6 + to AEM A	PADAREF	L48	48	O	ACD_NVETO_06AP	ACD_NVETO_06	L	LLDRV7, 3.5mA Max.LVDS Driver
56	Veto Ch 6 - to AEM A	PADAREF	L49	49	O	ACD_NVETO_06AM			
57	Veto Ch 6 + to AEM B	PADAREF	L50	50	O	ACD_NVETO_06BP	ACD_NVETO_06	L	LLDRV7, 3.5mA Max.LVDS Driver
58	Veto Ch 6 - to AEM B	PADAREF	L51	51	O	ACD_NVETO_06BM			
59	Digital Power	PADVdd	L52	52	P	DVDD			
60	Digital Ground	PADGnd	B1	53	P	DGND			

	A	B	C	D	F	G	H	I	K
61	Veto Ch 7 + to AEM A	PADAREF	B2	54	O	ACD_NVETO_07AP	ACD_NVETO_07	L	LLDRV7, 3.5mA Max.LVDS Driver
62	Veto Ch 7 - to AEM A	PADAREF	B3	55	O	ACD_NVETO_07AM			
63	Veto Ch 7 + to AEM B	PADAREF	B4	56	O	ACD_NVETO_07BP	ACD_NVETO_07	L	LLDRV7, 3.5mA Max.LVDS Driver
64	Veto Ch 7 - to AEM B	PADAREF	B5	57	O	ACD_NVETO_07BM			
65	Veto Ch 8 + to AEM A	PADAREF	B6	58	O	ACD_NVETO_08AP	ACD_NVETO_08	L	LLDRV7, 3.5mA Max.LVDS Driver
66	Veto Ch 8 - to AEM A	PADAREF	B7	59	O	ACD_NVETO_08AM			
67	Veto Ch 8 + to AEM B	PADAREF	B8	60	O	ACD_NVETO_08BP	ACD_NVETO_08	L	LLDRV7, 3.5mA Max.LVDS Driver
68	Veto Ch 8 - to AEM B	PADAREF	B9	61	O	ACD_NVETO_08BM			
69	Veto Ch 9 + to AEM A	PADAREF	B10	62	O	ACD_NVETO_09AP	ACD_NVETO_09	L	LLDRV7, 3.5mA Max.LVDS Driver
70	Veto Ch 9 - to AEM A	PADAREF	B11	63	O	ACD_NVETO_09AM			
71	Veto Ch 9 + to AEM B	PADAREF	B12	64	O	ACD_NVETO_09BP	ACD_NVETO_09	L	LLDRV7, 3.5mA Max.LVDS Driver
72	Veto Ch 9 - to AEM B	PADAREF	B13	65	O	ACD_NVETO_09BM			
73	Veto Ch 10 + to AEM A	PADAREF	B14	66	O	ACD_NVETO_10AP	ACD_NVETO_10	L	LLDRV7, 3.5mA Max.LVDS Driver
74	Veto Ch 10 - to AEM A	PADAREF	B15	67	O	ACD_NVETO_10AM			
75	Veto Ch 10 + to AEM B	PADAREF	B16	68	O	ACD_NVETO_10BP	ACD_NVETO_10	L	LLDRV7, 3.5mA Max.LVDS Driver
76	Veto Ch 10 - to AEM B	PADAREF	B17	69	O	ACD_NVETO_10BM			
77	Veto Ch 11 + to AEM A	PADAREF	B18	70	O	ACD_NVETO_11AP	ACD_NVETO_11	L	LLDRV7, 3.5mA Max.LVDS Driver
78	Veto Ch 11 - to AEM A	PADAREF	B19	71	O	ACD_NVETO_11AM			
79	Veto Ch 11 + to AEM B	PADAREF	B20	72	O	ACD_NVETO_11BP	ACD_NVETO_11	L	LLDRV7, 3.5mA Max.LVDS Driver
80	Veto Ch 11 - to AEM B	PADAREF	B21	73	O	ACD_NVETO_11BM			
81	Veto Ch 12 + to AEM A	PADAREF	B22	74	O	ACD_NVETO_12AP	ACD_NVETO_12	L	LLDRV7, 3.5mA Max.LVDS Driver

	A	B	C	D	F	G	H	I	K
82	Veto Ch 12 - to AEM A	PADAREF	B23	75	O	ACD_NVETO_12AM			
83	Veto Ch 12 + to AEM B	PADAREF	B24	76	O	ACD_NVETO_12BP	ACD_NVETO_12	L	LLDRV7, 3.5mA Max.LVDS Driver
84	Veto Ch 12 - to AEM B	PADAREF	B25	77	O	ACD_NVETO_12BM			
85	Digital Power	PADVdd	B26	78	P	DVDD			
86	GAFE 17 PHA Channel ID	PADAREF	B27	79	I	CHID_17	CHID_17_IN	H	RCVRF, 502 Ohms to IRTN, pseudo LVDS
87	Digital Ground	PADGnd	B28	80	P	DGND			
88	GAFE 17 VETO Discriminator	PADAREF	B29	81	I	DISC_17	DISC_17_IN	H	RCVRF, 502 Ohms to IRTN, pseudo LVDS
89	GAFE 17 Current Return	PADAREF	B30	82	R	IRTN_17			
90	GAFE 16 PHA Channel ID	PADAREF	B31	83	I	CHID_16	CHID_16_IN	H	RCVRF, 502 Ohms to IRTN, pseudo LVDS
91	GAFE 16 VETO Discriminator	PADAREF	B32	84	I	DISC_16	DISC_16_IN	H	RCVRF, 502 Ohms to IRTN, pseudo LVDS
92	GAFE 16 Current Return	PADAREF	B33	85	R	IRTN_16			
93	GAFE 15 PHA Channel ID	PADAREF	B34	86	I	CHID_15	CHID_15_IN	H	RCVRF, 502 Ohms to IRTN, pseudo LVDS
94	GAFE 15 VETO Discriminator	PADAREF	B35	87	I	DISC_15	DISC_15_IN	H	RCVRF, 502 Ohms to IRTN, pseudo LVDS
95	GAFE 15 Current Return	PADAREF	B36	88	R	IRTN_15			
96	GAFE 14 PHA Channel ID	PADAREF	B37	89	I	CHID_14	CHID_14_IN	H	RCVRF, 502 Ohms to IRTN, pseudo LVDS
97	GAFE 14 VETO Discriminator	PADAREF	B38	90	I	DISC_14	DISC_14_IN	H	RCVRF, 502 Ohms to IRTN, pseudo LVDS
98	GAFE 14 Current Return	PADAREF	B39	91	R	IRTN_14			
99	GAFE 13 PHA Channel ID	PADAREF	B40	92	I	CHID_13	CHID_13_IN	H	RCVRF, 502 Ohms to IRTN, pseudo LVDS
100	GAFE 13 VETO Discriminator	PADAREF	B41	93	I	DISC_13	DISC_13_IN	H	RCVRF, 502 Ohms to IRTN, pseudo LVDS
101	GAFE 13 Current Return	PADAREF	B42	94	R	IRTN_13			
102	GAFE 12 PHA Channel ID	PADAREF	B43	95	I	CHID_12	CHID_12_IN	H	RCVRF, 502 Ohms to IRTN, pseudo LVDS

	A	B	C	D	F	G	H	I	K
103	GAFE 12 VETO Discriminator	PADAREF	B44	96	I	DISC_12	DISC_12_IN	H	RCVRF, 502 Ohms to IRTN, pseudo LVDS
104	GAFE 12 Current Return	PADAREF	B45	97	R	IRTN_12			
105	GAFE 11 PHA Channel ID	PADAREF	B46	98	I	CHID_11	CHID_11_IN	H	RCVRF, 502 Ohms to IRTN, pseudo LVDS
106	GAFE 11 VETO Discriminator	PADAREF	B47	99	I	DISC_11	DISC_11_IN	H	RCVRF, 502 Ohms to IRTN, pseudo LVDS
107	GAFE 11 Current Return	PADAREF	B48	100	R	IRTN_11			
108	GAFE 10 PHA Channel ID	PADAREF	B49	101	I	CHID_10	CHID_10_IN	H	RCVRF, 502 Ohms to IRTN, pseudo LVDS
109	GAFE 10 VETO Discriminator	PADAREF	B50	102	I	DISC_10	DISC_10_IN	H	RCVRF, 502 Ohms to IRTN, pseudo LVDS
110	GAFE 10 Current Return	PADAREF	B51	103	R	IRTN_10			
111	HLD Wor Receiver Bias Adjust	PADAREF	B52	104	B	HLD_WOR_BIAS			WOR_BIAS, 7k Ohm to ground
112	GAFE 9 PHA Channel ID	PADAREF	R52	105	I	CHID_09	CHID_09_IN	H	RCVRF, 502 Ohms to IRTN, pseudo LVDS
113	GAFE 9 VETO Discriminator	PADAREF	R51	106	I	DISC_09	DISC_09_IN	H	RCVRF, 502 Ohms to IRTN, pseudo LVDS
114	GAFE 9 Current Return	PADAREF	R50	107	R	IRTN_09			
115	GAFE 8 PHA Channel ID	PADAREF	R49	108	I	CHID_08	CHID_08_IN	H	RCVRF, 502 Ohms to IRTN, pseudo LVDS
116	GAFE 8 VETO Discriminator	PADAREF	R48	109	I	DISC_08	DISC_08_IN	H	RCVRF, 502 Ohms to IRTN, pseudo LVDS
117	GAFE 8 Current Return	PADAREF	R47	110	R	IRTN_08			
118	GAFE 7 PHA Channel ID	PADAREF	R46	111	I	CHID_07	CHID_07_IN	H	RCVRF, 502 Ohms to IRTN, pseudo LVDS
119	GAFE 7 VETO Discriminator	PADAREF	R45	112	I	DISC_07	DISC_07_IN	H	RCVRF, 502 Ohms to IRTN, pseudo LVDS
120	GAFE 7 Current Return	PADAREF	R44	113	R	IRTN_07			
121	GAFE 6 PHA Channel ID	PADAREF	R43	114	I	CHID_06	CHID_06_IN	H	RCVRF, 502 Ohms to IRTN, pseudo LVDS
122	GAFE 6 VETO Discriminator	PADAREF	R42	115	I	DISC_06	DISC_06_IN	H	RCVRF, 502 Ohms to IRTN, pseudo LVDS
123	GAFE 6 Current Return	PADAREF	R41	116	R	IRTN_06			

	A	B	C	D	F	G	H	I	K
124	GAFE 5 PHA Channel ID	PADAREF	R40	117	I	CHID_05	CHID_05_IN	H	RCVRF, 502 Ohms to IRTN, pseudo LVDS
125	GAFE 5 VETO Discriminator	PADAREF	R39	118	I	DISC_05	DISC_05_IN	H	RCVRF, 502 Ohms to IRTN, pseudo LVDS
126	GAFE 5 Current Return	PADAREF	R38	119	R	IRTN_05			
127	GAFE 4 PHA Channel ID	PADAREF	R37	120	I	CHID_04	CHID_04_IN	H	RCVRF, 502 Ohms to IRTN, pseudo LVDS
128	GAFE 4 VETO Discriminator	PADAREF	R36	121	I	DISC_04	DISC_04_IN	H	RCVRF, 502 Ohms to IRTN, pseudo LVDS
129	GAFE 4 Current Return	PADAREF	R35	122	R	IRTN_04			
130	GAFE 3 PHA Channel ID	PADAREF	R34	123	I	CHID_03	CHID_03_IN	H	RCVRF, 502 Ohms to IRTN, pseudo LVDS
131	GAFE 3 VETO Discriminator	PADAREF	R33	124	I	DISC_03	DISC_03_IN	H	RCVRF, 502 Ohms to IRTN, pseudo LVDS
132	GAFE 3 Current Return	PADAREF	R32	125	R	IRTN_03			
133	GAFE 2 PHA Channel ID	PADAREF	R31	126	I	CHID_02	CHID_02_IN	H	RCVRF, 502 Ohms to IRTN, pseudo LVDS
134	GAFE 2 VETO Discriminator	PADAREF	R30	127	I	DISC_02	DISC_02_IN	H	RCVRF, 502 Ohms to IRTN, pseudo LVDS
135	GAFE 2 Current Return	PADAREF	R29	128	R	IRTN_02			
136	GAFE 1 PHA Channel ID	PADAREF	R28	129	I	CHID_01	CHID_01_IN	H	RCVRF, 502 Ohms to IRTN, pseudo LVDS
137	GAFE 1 VETO Discriminator	PADAREF	R27	130	I	DISC_01	DISC_01_IN	H	RCVRF, 502 Ohms to IRTN, pseudo LVDS
138	GAFE 1 Current Return	PADAREF	R26	131	R	IRTN_01			
139	Digital Power	PADVdd	R25	132	P	DVDD			
140	GAFE 0 PHA Channel ID	PADAREF	R24	133	I	CHID_00	CHID_00_IN	H	RCVRF, 502 Ohms to IRTN, pseudo LVDS
141	GAFE 0 VETO Discriminator	PADAREF	R23	134	I	DISC_00	DISC_00_IN	H	RCVRF, 502 Ohms to IRTN, pseudo LVDS
142	GAFE 0 Current Return	PADAREF	R22	135	R	IRTN_00			
143	Digital Ground	PADGnd	R21	136	P	DGND			
144	GAFE 17 ADC PHA Data	PADInC	R20	137	I	PHAD_17	PHAD_17_IN	H	5pF Load

	A	B	C	D	F	G	H	I	K
145	GAFE 16 ADC PHA Data	PADInC	R19	138	I	PHAD_16	PHAD_16_IN	H	5pF Load
146	GAFE 15 ADC PHA Data	PADInC	R18	139	I	PHAD_15	PHAD_15_IN	H	5pF Load
147	GAFE 14 ADC PHA Data	PADInC	R17	140	I	PHAD_14	PHAD_14_IN	H	5pF Load
148	GAFE 13 ADC PHA Data	PADInC	R16	141	I	PHAD_13	PHAD_13_IN	H	5pF Load
149	GAFE 12 ADC PHA Data	PADInC	R15	142	I	PHAD_12	PHAD_12_IN	H	5pF Load
150	GAFE 11 ADC PHA Data	PADInC	R14	143	I	PHAD_11	PHAD_11_IN	H	5pF Load
151	GAFE 10 ADC PHA Data	PADInC	R13	144	I	PHAD_10	PHAD_10_IN	H	5pF Load
152	GAFE 9 ADC PHA Data	PADInC	R12	145	I	PHAD_09	PHAD_09_IN	H	5pF Load
153	GAFE 8 ADC PHA Data	PADInC	R11	146	I	PHAD_08	PHAD_08_IN	H	5pF Load
154	GAFE 7 ADC PHA Data	PADInC	R10	147	I	PHAD_07	PHAD_07_IN	H	5pF Load
155	GAFE 6 ADC PHA Data	PADInC	R9	148	I	PHAD_06	PHAD_06_IN	H	5pF Load
156	GAFE 5 ADC PHA Data	PADInC	R8	149	I	PHAD_05	PHAD_05_IN	H	5pF Load
157	GAFE 4 ADC PHA Data	PADInC	R7	150	I	PHAD_04	PHAD_04_IN	H	5pF Load
158	GAFE 3 ADC PHA Data	PADInC	R6	151	I	PHAD_03	PHAD_03_IN	H	5pF Load
159	GAFE 2 ADC PHA Data	PADInC	R5	152	I	PHAD_02	PHAD_02_IN	H	5pF Load
160	GAFE 1 ADC PHA Data	PADInC	R4	153	I	PHAD_01	PHAD_01_IN	H	5pF Load
161	GAFE 0 ADC PHA Data	PADInC	R3	154	I	PHAD_00	PHAD_00_IN	H	5pF Load
162	Digital Power	PADVdd	R2	155	P	DVDD			
163	LVDS receiver biasing Adjust	PADAREF	R1	156	B	BIAS_RCVR			RCVR_BIAS, 84k Ohm to DVDD
164	Digital Ground	PADGnd	T52	157	P	DGND			
165	HLD Current Return	PADAREF	T51	158	R	IRTN_HL_DISC			

	A	B	C	D	F	G	H	I	K
166	HLD OR'ed Signal	PADAREF	T50	159	I	OR_HL_DISC	HLD_OR_IN	H	WOR_RCVR, 788 Ohms between P and M
167	LVDS 7mA drivers biasing	PADAREF	T49	160	B	BIAS_DRV_H			LL_BIAS, for LLDRV7's, 7k Ohm to ground
168	GAFE Hold +	PADAREF	T48	161	O	GAFE_HOLDP	GAFE_HOLD	H	LLDRV4, 2.0mA Max. LVDS Driver
169	GAFE Hold -	PADAREF	T47	162	O	GAFE_HOLDM			
170	GAFE Strobe +	PADAREF	T46	163	O	GAFE_STROBEP	GAFE_STROBE	H	LLDRV4, 2.0mA Max. LVDS Driver
171	GAFE Strobe -	PADAREF	T45	164	O	GAFE_STROBEM			
172	GAFE Configuration Data +	PADAREF	T44	165	O	GAFE_DATP	GAFE_DAT	H	LLDRV4, 2.0mA Max. LVDS Driver
173	GAFE Configuration Data -	PADAREF	T43	166	O	GAFE_DATM			
174	GAFE Configuration Clock +	PADAREF	T42	167	O	GAFE_CLKP	GAFE_CLK	H	LLDRV4, 2.0mA Max. LVDS Driver
175	GAFE Configuration Clock -	PADAREF	T41	168	O	GAFE_CLKM			
176	LVDS 2mA drivers biasing	PADAREF	T40	169	B	BIAS_DRV_L			LL_BIAS, for LLDRV4's, 7k Ohm to ground
177	GAFE Return Data	PADInC	T39	170	I	GAFE_RET_DATA	GAFE_RET_DAT	H	5pF Load
178	GAFE Reset	PadOut	T38	171	O	GAFE_RST	GAFE_RST_OUT	H	Can drive 14pF at 500pS
179	ADC Clock	PADOut	T37	172	O	ADC_CLK	ADC_CLK_OUT	H	Can drive 14pF at 500pS
180	ADC Chip Select	PADOut	T36	173	O	NADC_CS	NADC_CS_OUT	L	Can drive 14pF at 500pS
181	MAX5121 Configuration Clock	PADOut	T35	174	O	DAC_CLK	DAC_CLK_OUT	H	Can drive 14pF at 500pS
182	MAX5121 Configuration Data	PADOut	T34	175	O	DAC_DATA	DAC_DAT_RET	H	Can drive 14pF at 500pS
183	MAX5121 Readback Data	PADInC	T33	176	I	DAC_READBACK	DAC_DATA_OUT	H	5pF Load
184	MAX5121 Chip Select	PADOut	T32	177	O	NDAC_CS	NDAC_CS_OUT	L	Can drive 14pF at 500pS
185	Max5121 Chip Reset	PADOut	T31	178	O	NDAC_CLR	NDAC_CLR_OUT	L	Can drive 14pF at 500pS
186	GARC Test Bus Signal 1	PADOut	T30	179	O	HITMAP_TEST	HITMAP_TEST_OUT	H	Can drive 14pF at 500pS

	A	B	C	D	F	G	H	I	K
187	GARC Test Bus Signal 2	PADOut	T29	180	O	TRIG_TST	TRIGGER_OUT	H	Can drive 14pF at 500pS
188	GARC Test Bus Signal 3	PADInC	T28	181	I	FREE_ID	FREE_ID_IN	H	5pF Load
189	GARC Power-on reset input	PADInC	T27	182	I	PWR_ON_RST	PWR_ON_RST_IN	H	5pF Load
190	GARC Test Bus Signal 4	PADOut	T26	183	O	VETO_ENA_TST	VETO_ENA_OUT	H	Can drive 14pF at 500pS
191	LVDS Preset current Adjust Pin	PADAREF	T25	184	B	LVDS_PRESETADJ	LVDS_PRESETADJ		7k to DVDD
192	HV Enable, HVBS Prime	PADOut	T24	185	O	HV_ENABLE_1	HV_ENABLE_1OUT	H	
193	HV Enable, HVBS Redundant	PADOut	T23	186	O	HV_ENABLE_2	HV_ENABLE_2OUT	H	Can drive 14pF at 500pS
194	Digital Ground	PADGnd	T22	187	P	DGND			
195	Veto Ch 17 + to AEM A	PADAREF	T21	188	O	ACD_NVETO_17AP	ACD_NVETO_17	L	LLDRV7, 3.5mA Max.LVDS Driver
196	Veto Ch 17 - to AEM A	PADAREF	T20	189	O	ACD_NVETO_17AM			
197	Veto Ch 17 + to AEM B	PADAREF	T19	190	O	ACD_NVETO_17BP	ACD_NVETO_17	L	LLDRV7, 3.5mA Max.LVDS Driver
198	Veto Ch 17 - to AEM B	PADAREF	T18	191	O	ACD_NVETO_17BM			
199	Veto Ch 16 + to AEM A	PADAREF	T17	192	O	ACD_NVETO_16AP	ACD_NVETO_16	L	LLDRV7, 3.5mA Max.LVDS Driver
200	Veto Ch 16 - to AEM A	PADAREF	T16	193	O	ACD_NVETO_16AM			
201	Veto Ch 16 + to AEM B	PADAREF	T15	194	O	ACD_NVETO_16BP	ACD_NVETO_16	L	LLDRV7, 3.5mA Max.LVDS Driver
202	Veto Ch 16 - to AEM B	PADAREF	T14	195	O	ACD_NVETO_16BM			
203	Veto Ch 15 + to AEM A	PADAREF	T13	196	O	ACD_NVETO_15AP	ACD_NVETO_15	L	LLDRV7, 3.5mA Max.LVDS Driver
204	Veto Ch 15 - to AEM A	PADAREF	T12	197	O	ACD_NVETO_15AM			
205	Veto Ch 15 + to AEM B	PADAREF	T11	198	O	ACD_NVETO_15BP	ACD_NVETO_15	L	LLDRV7, 3.5mA Max.LVDS Driver
206	Veto Ch 15 - to AEM B	PADAREF	T10	199	O	ACD_NVETO_15BM			
207	Veto Ch 14 + to AEM A	PADAREF	T9	200	O	ACD_NVETO_14AP	ACD_NVETO_14	L	LLDRV7, 3.5mA Max.LVDS Driver

	A	B	C	D	F	G	H	I	K
208	Veto Ch 14 - to AEM A	PADAREF	T8	201	O	ACD_NVETO_14AM			
209	Veto Ch 14 + to AEM B	PADAREF	T7	202	O	ACD_NVETO_14BP	ACD_NVETO_14	L	LLDRV7, 3.5mA Max.LVDS Driver
210	Veto Ch 14 - to AEM B	PADAREF	T6	203	O	ACD_NVETO_14BM			
211	Veto Ch 13 + to AEM A	PADAREF	T5	204	O	ACD_NVETO_13AP	ACD_NVETO_13	L	LLDRV7, 3.5mA Max.LVDS Driver
212	Veto Ch 13 - to AEM A	PADAREF	T4	205	O	ACD_NVETO_13AM			
213	Veto Ch 13 + to AEM B	PADAREF	T3	206	O	ACD_NVETO_13BP	ACD_NVETO_13	L	LLDRV7, 3.5mA Max.LVDS Driver
214	Veto Ch 13 - to AEM B	PADAREF	T2	207	O	ACD_NVETO_13BM			
215	Digital Power	PADVdd	T1	208	P	DVDD			
216	Global reset input (from core gen. Reset_out)			CORE	Core Input		N_G_RESET	L	GLOBAL RESET BUS FOR CORE
217	Reset Output (generated in the core)			CORE	Core Output		NRESET_OUT	L	Into a 2 x BUF4 and 575xbuf1's into N_G_RESET to Drive Global Reset Bus
218	Output of clock buffer into Core module			CORE	Core Input		ACD_CLK	H	Global clock for core
219	Selected Clock from Core to clock buffer			CORE	Core Output		CLK_OUT	H	Into 4 x BUF4's into 36 x BUF4's into 557 BUF1's t Drive Global ACD_CLK of Core
220	INPUT HIGH			CORE	Core Input		HI_INPUT	H	Tie-High