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GLAST Large Area Telescope (LAT) Anti-Coincidence Detector (ACD)



Electronics Specifications

DRAFT

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1 Introduction

The Gamma-ray Large Area Space Telescope (GLAST) will study the cosmos in the energy range 10 keV to 300 GeV. GLAST will be a flexible observatory for investigating the great range of astrophysical phenomena best studied in high-energy gamma rays.

The GLAST will have an imaging gamma-ray telescope vastly more capable than instruments flown previously, as well as a secondary instrument to augment the study of transient gamma ray events. The main instrument of GLAST, the Large Area Telescope (LAT), will have superior area, angular resolution, field of view, and dead-time that together will provide a factor of 30 or more advance in sensitivity over that of previous missions, as well as providing the capability for study of gamma-ray bursts. The LAT will operate in the range of 20 MeV - 300 GeV.

The anticipated advances in astronomy and high-energy physics with GLAST are among the central subjects of NASA's Structure and Evolution of the Universe (SEU) research theme and the Department of Energy's non-accelerator research program. NASA recognizes the scientific goals of the GLAST mission as part of the SEU Cosmic Journeys planned for the study of black holes and dark matter. The physics and astrophysics programs in the partner countries of France, Germany, Italy, Japan, and Sweden also support the GLAST mission. NASA plans to launch GLAST in 2006.

1.1 Purpose and Scope

The LAT is a pair conversion gamma-ray telescope. The Anticoincidence Detector (ACD) is a major subsystem of the LAT. The ACD provides the capability to distinguish the charged particle background from the gamma-rays of interest with high efficiency. A secondary function of the ACD is to identify the passage of heavy nuclei through the LAT, for use in calibrating the Calorimeter Subsystem.

This document describes the electronics specifications for the ACD subsystem electronics, relating the electronics design to the Level III LAT ACD requirements, LAT-SS-00016, the Level IV ACD Requirements, LAT-SS-00352, and additional documents detailed in the following sections.

1.2 Anti-Coincidence Detector (ACD) Electronics Overview

The primary interaction of photons with matter in the GLAST LAT energy range is pair conversion. Pair conversion forms the basis for the underlying measurement principle by providing a unique signature for gamma rays. A reconstruction of the trajectories of the resultant positron and electron pairs allows determination of the incident photon direction.

Since the cosmic charged particle background flux is up to 10^4 times larger than that of gamma rays in the GLAST energy range, it is important to eliminate the great majority of these events from the LAT data processing. The ACD consists of scintillating tiles that respond to the incident charged particles but are insensitive to gamma rays. Photons generated in the scintillators, by the passage of charged particles, are optically collected and converted to electrical signals via photomultiplier tubes that are attached to the tiles. The output current of each photomultiplier tube is amplified and conditioned prior to a measurement of the signal amplitude. A series of discriminators is used for a wide-bandwidth amplitude determination, and the analog input signal is shaped for a more precise pulse height measurement. Digital data are captured from these analog chains via LAT command. These data are formatted and telemetered to the LAT computer for filtering, commutation, and downlink.

This document describes the LAT ACD electronics specifications and relates the electronics specifications to the ACD electronics requirements.

2 Definitions

2.1 Acronyms

ACD - Anti-Coincidence Detector
ADC - analog-to-digital converter
AEM - ACD Electronics Module
ASIC - application specific integrated circuit
dB - decibel
C - degrees Celsius
CAL – Calorimeter
CMD - command
DNL - Differential Non-Linearity
FSM – Finite State Machine
GLAST - Gamma-ray Large Area Space Telescope
GeV – Gigaelectron volts
gm - grams
HLD - High Level Discriminator
I - current in amps
I-V – current to voltage conversion
INL - Integral Non-Linearity
kg – kilograms
keV – kiloelectron volts
k Ω - kilohms
LAT - Large Area Telescope
LLD - Low Level Discriminator
L1T - Level 1 Trigger Acknowledge
 μ A - microamps
mA - milliamps
mV - millivolts
mW - milliwatts
MIP - minimum ionizing (singly-charged) particle, or the signal(s) it produces
MTTF - Mean Time to Failure
NIM - nuclear instrumentation standard
PCB - printed circuit board
PHA - Pulse Height Amplitude
PMT - Photomultiplier Tube
p-p - peak-to-peak.
RMS - Root Mean Square; (or voltage 1mV RMS == 2.828 mV p-p)
SEU - single event upset
TBD - to be determined
TBR - to be resolved
TKR - Tracker
V – volts

2.2 Definitions

dB (voltage) : 1 dB = 20 log (V2/V1)

dB (power) : 1 dB = 10 log (P2/P1)

DNL - Differential Non-Linearity is used to describe the deviations between the measured and the ideal 1 LSB change of transition voltages in the ADC's transfer characteristic. The code width of the converter represents the span of input voltage which results in a given quantization level. This is a measure of the local slope error of the converter. For the ACD electronics using an 11-bit converter, the DNL will be defined per the following equation:

$$DNL(\%) = \left(\frac{T_{n+1} - T_n}{V_{FS} / 2^{11}} - 1 \right) * 100\%$$

Where T_n is the transition voltage of the n^{th} quantization level.

INL - Integral Non-Linearity is the measure of the maximum deviation of the actual transition points recorded by the ADC from a straight line drawn between the end points. The INL at the converter output is the sum of the integral non-linearity's of the analog chain. For this measurement, offset and gain errors are not included. For the ACD electronics, this measurement will be computed via a best-fit line as determined by a least squares fit algorithm, minimizing the error between the ACD data and a straight line. Allowing C_i to be the output code from a voltage input V_i , we get a line with slope m and intercept b from:

$$\begin{aligned} \bar{C} &= \frac{1}{n} \sum C_i \\ \bar{V} &= \frac{1}{n} \sum V_i \\ m &= \frac{\left[\sum C_i (V_i - \bar{V}) \right]}{\left[\sum (V_i - \bar{V})^2 \right]} \\ b &= \bar{C} - m\bar{V} \end{aligned}$$

where \bar{C} is the mean input value and \bar{V} is the mean output value.

Latchup - a change of state and loss of functionality (possibly permanently) induced when an energetic particle deposits sufficient energy to forward bias a parasitic pnpn silicon controlled rectifier, which is often generated in CMOS well processes. This may occur through direct ionization via galactic cosmic rays or by indirect ionization via protons.

Linear Energy Transfer (LET) - a measure of the energy deposited per unit length as an energetic particle travels through a material. The common LET unit is MeV*cm²/mg of silicon.

Power-on - the time that stable power at the proper voltage levels is applied to the ACD interface connector.

Single Fault Tolerant - A system is single fault tolerant if it may sustain any one failure without transitioning to a non-functional state. Common mode failures are excluded from this definition.

Unsafe State - a state or mode for the electronics that is either unknown or damaging to the electronics or another portion of the instrument.

3 Applicable Documents

- LAT-SS-00016-D10, "LAT ACD Subsystem Specification, Level III Specification"
- LAT-MD-00099-1, LAT Parts Program Control Plan
- LAT-SS-00352-D6, "LAT ACD Subsystem Specification - Level IV Electronics Requirements"
- LAT-SS-00363-Dx, "LAT Dataflow Subsystem Specification – ACD-AEM Interface".
- LAT-MD-00066-1, LAT System Engineering Management Plan
- LAT-SS-00010-01, LAT Performance Specification
- LAT EMI/EMC Document, [TBD System Engineer](#)
- Grounding requirements [TBD Shibleie/Amato/Unger](#)
- NASA-STD-8739.1, Workmanship Standards for Staking and Conformal Coating of Printed Wiring Boards and Electronic Assemblies
- Test requirements [TBD System Engineer](#)

4 Level V Requirements

4.1 Requirement for ASICs

The need for custom-designed ASICs is a derived requirement from the power, radiation tolerance/SEU, number of analog electronics channels, and volume allocations for the ACD. Accomplishment of the ACD front-end requirements with discrete electronic components is not viable. The requirements are derived from the LAT ACD Electronics Level IV requirements, LAT-SS-00352, and the LAT ACD–AEM Interface Control Document, LAT-SS-00363.

4.2 Reliability Requirements for the Electronics

The ACD electronics will be single fault tolerant with no complete loss of signal from a tile in the event of the first failure. [LAT-SS-00352, section 5.13.1]. The ACD electronics will be designed for a minimum on-orbit lifetime of 5 years. [LAT-SS-00352, section 5.19] The ACD electronics reliability will be estimated via calculation. The ACD hardware time-variable reliability function, $R(t)$, is assumed to be of the exponential form given below:

$$R(t) = e^{-\lambda t}$$

Section 5.13.2 of LAT-SS-00352 states that the probability of the loss of both VETO signals from a single scintillator tile shall be less than 1% per year. This specification addresses failures only, not degradation.

For two photomultiplier tube channels in parallel, this implies the following reliability requirement for each of the two channels:

$$R(t = 1 \text{ yr}) = e^{-\lambda t} \Rightarrow (1-0.01)^2 \approx 0.9801, \text{ or } \lambda = -\ln(0.9801) = 0.02$$

The maximum allowable failure rate for the ACD channel, λ , is thus 0.02 per year. The MTTF for this rate is $1/\lambda \sim 50$ years.

4.3 Parts Selection and Packaging Requirements

The GLAST LAT Project Parts Engineer (PPE) has responsibility for the parts program. Whenever possible, as determined by the ACD Lead Electronics Engineer, parts will be selected from the NASA Parts Selection List (NPSL) or the GSFC PPL-21. The NPSL and PPL parts have established procurement specifications, multiple sources of supply, and have been assessed for quality, reliability, and risk in spaceflight applications. Due to the requirements of ACD, however, there will be several parts required for the design that are not available from the NPSL, including the custom ASICs.

Parts not from the NPSL will be subject to the parts qualification program detailed by LAT-MD-00099-1. In some areas of the ACD FREE circuit card, due to power and PCB area restrictions, the use of surface mount PEM devices is indicated instead of traditional hermetically packaged parts. Whenever possible, the ACD team will utilize packaging strategies and implementation methods similar to the other LAT subsystems.

5 Anti-Coincidence Detector (ACD) Electronics

The GLAST LAT ACD electronics is used to provide charge collection, amplification and signal processing for the ACD scintillating tiles. The ACD interfaces to the AEM as a subsystem of the LAT. The primary function of the ACD subsystem is to differentiate charged particle passage from gamma-ray photons. This is done by means of scintillating plastic tiles, photomultiplier tubes, and signal processing electronics. [Ref. LAT-SS-00016, 5.1].

There are 89 plastic scintillator tiles - 25 on the LAT top and 16 on each of the four sides. Eight scintillating fiber ribbons cover the gaps between the tiles. There are two photomultiplier tubes per tile. [Ref. LAT-SS-00016, 5.1]

ACD Electronics Assembly	Predominant Circuitry Type	Number of Assemblies Required for Flight Unit
High Voltage Bias Supplies	Analog/Power (PMT bias)	24
Resistor Networks	Analog	194
FREE circuit card (18 channels per board)	Analog and Digital	12
Photomultiplier Tubes	Analog	194

5.1 ACD System

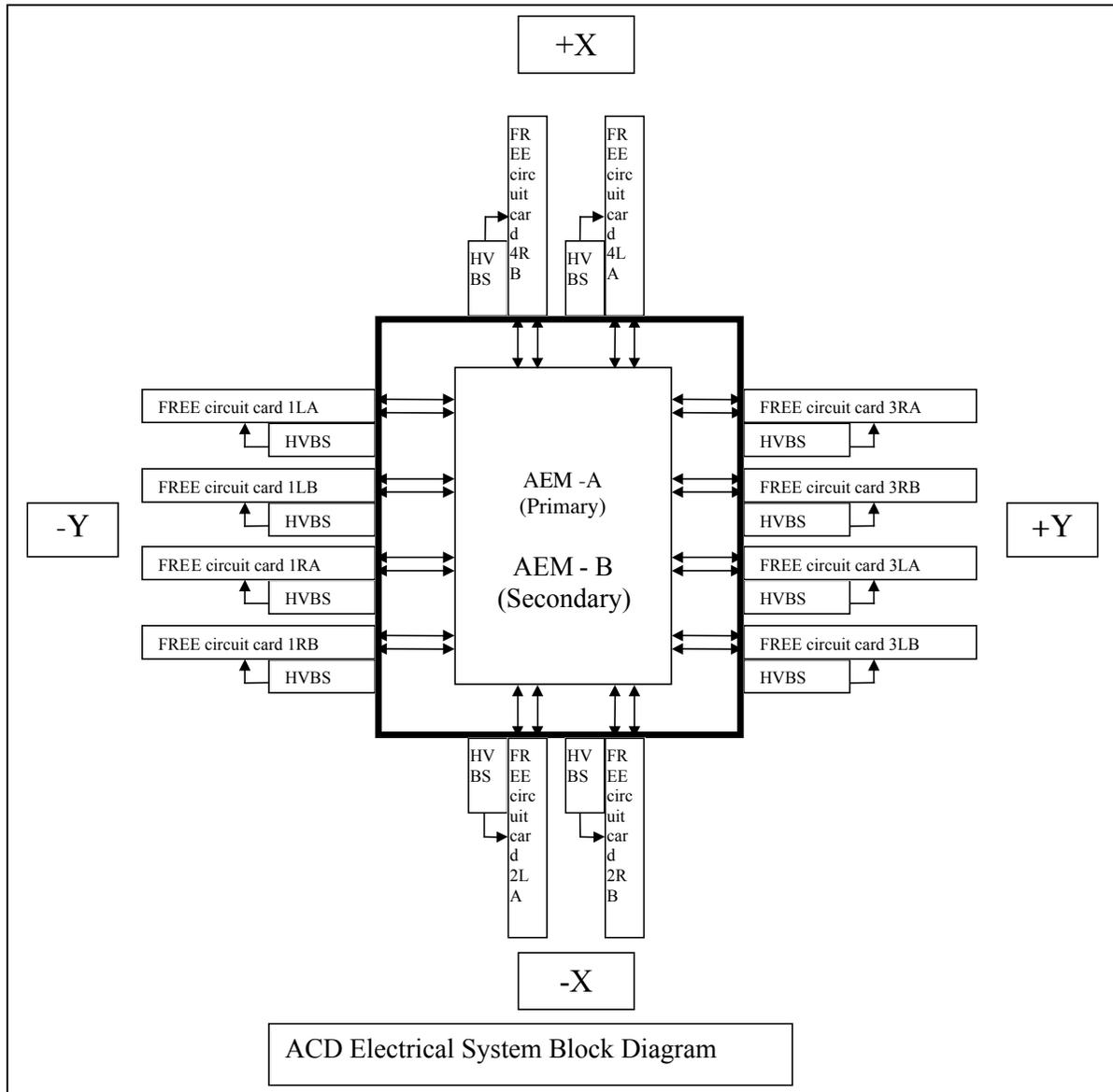
The block diagram below shows the arrangement of the 12 ACD Front-End Electronics (FREE) circuit cards and their positions around the Base Electronics Assembly (BEA). The BEA has eight bays, two on each side. Each bay can house up to two FREE cards, four High Voltage Bias Supplies (HVBS), and 36 PhotoMultiplier Tubes (PMTs). The ACD is covered on five sides by 89 scintillator tiles. Each tile outputs identical optical signals to two PMT, via wave shifting fiber and clear fiber. Also, there are eight scintillating fiber ribbons, with two PMTs per ribbon. In the current design, +Y and -Y sides of the ACD house 72 PMTs and the +X and -X sides house 36 PMTs each, for a system total of 216 analog chains. The FREE cards interconnect directly to the AEM via a 79-pin connector. There is no interconnection between FREE cards. There are no trigger primitives generated at the ACD.

- 18 PMT Channels per FREE circuit card

- 12 FREE circuit card per ACD system
- 216 Total Channels available

5.1.1 Electronics Design Responsibilities

WBS #	Design Task	Responsibility
	High Voltage Bias Supply	Art Ruitberg
	High Voltage Resistor Network	Art Ruitberg
	Photomultiplier Tubes	Bob Hartman
	ACD FREE circuit card	Dave Sheppard and Bob Baker
	Analog ASIC design	Gunther Haller
	Analog ASIC test	Chandru Mirchandani
	Digital ASIC	Dave Sheppard and Bob Baker
	AEM Eng. Model (5)	SLAC / Haller
	Flight Harness	SLAC / Haller



In The boards are located according to the following plan:

ACD FREE circuit Card	LAT Location
FREE circuit card 1LA, 1LB	-? side
FREE circuit card 1RA, 1RB	-? side
FREE circuit card 2LA, 2RB	-? side
FREE circuit card 3LA, 3LB	+? side
FREE circuit card 3RA, 3RB	+? side
FREE circuit card 4LA, 4RB	+? side

5.1.2 Electronics Enclosures

The ACD electronics will be fully enclosed in conductive housings. These housings will provide protection for the electronics and act as faraday cages for radiative emissions and susceptibility. Part or all of these enclosures will be plated with a non-oxidizing, conductive passivation to ensure grounding to the ACD chassis. The BEA mechanical structure is considered ACD chassis. The ACD electronics enclosures will provide a minimum of 0.05" of aluminum (or equivalent) for protection from both micrometeoroids and space debris, and for the reduction of the total dose of ionizing radiation.

5.1.3 Electronics Power Dissipation

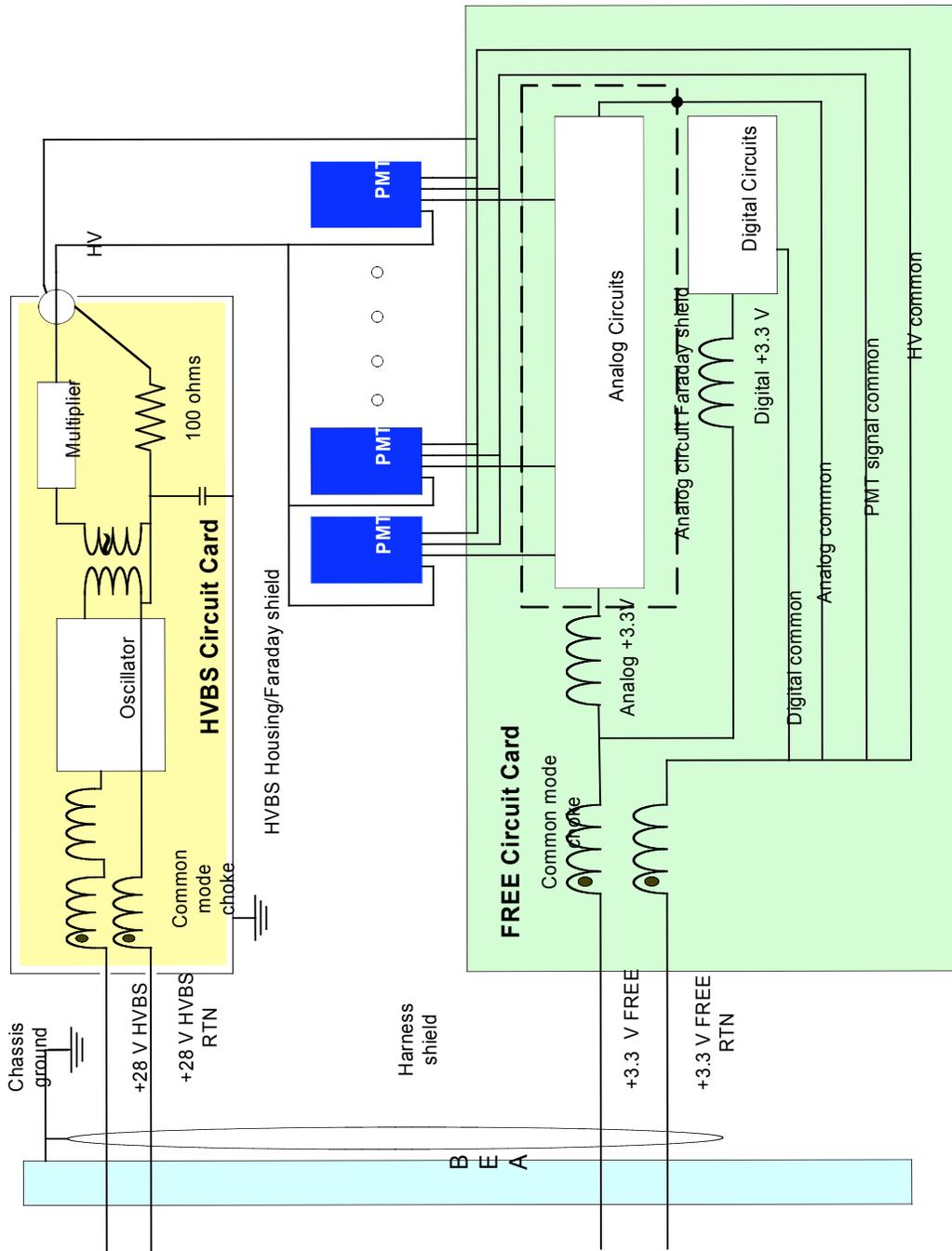
The total power dissipated by the ACD electronics, excluding heater circuitry, shall be less than 37 watts, as defined by LAT-SS-00016 and LAT-SS-00352, section 5.16. The total power dissipated by each ACD FREE circuit card and HVBS will be no more than 2.25 watts.

5.1.4 Electronics Mass

Electronics board mass is estimated using 8 grams per square inch. The mass of an ACD FREE circuit card will not exceed 600 gm. The mass of the enclosure is not included in this estimate. The total mass of the ACD electronics will not exceed **25 kilograms, excluding the external wiring harnessing to the AEM, as per LAT-SS-00352, section 5.17.**

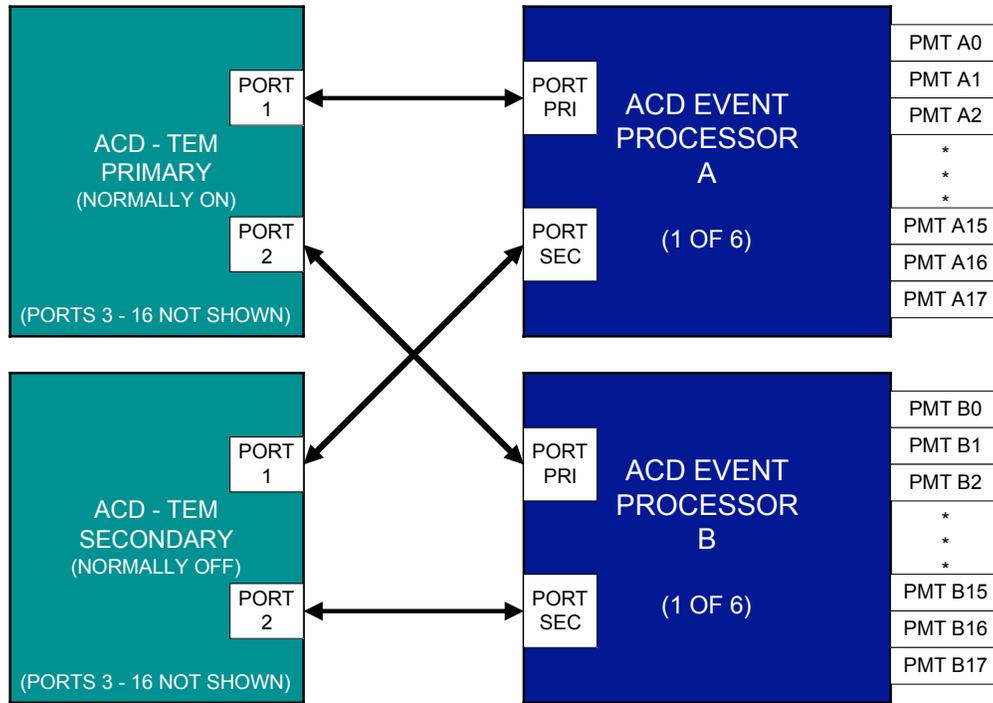
5.1.5 System Grounding Diagram

The ACD electronics maintains two grounds on the FREE circuit card, the analog ground and the digital ground. These grounds are isolated from the ACD chassis in an effort to preclude ground currents in the structure. The +28V will be used for the operation of the HVBS. The HVBS output will be referenced to the analog ground at the analog ASIC. This analog ground will be isolated from the HVBS ground and the 28V RTN, by a 100-ohm resistor. Common mode chokes are used on each power rail input. The analog and digital grounds are common on the LAT interface side of the common mode chokes. The common ground shall be tied to ACD chassis at the LAT.



5.1.6 Electronics Cross-Strapping

There will be cross-strapping of electronics at the AEM for redundancy to improve system reliability. This will be implemented in the following manner:



Electronics Cross-Strapping

5.1.7 Number of Analog Electronics Channels

There are 89 scintillating tiles with two PMTs per tile, plus 16 PMTs reading out 8 scintillating fiber ribbons. There will be a separate analog processing chain per PMT for a total of 194 analog processing channels required.

5.1.8 Definition of a Minimum Ionizing Particle

The definition of a Minimum Ionizing Particle (MIP) must be normalized to an equivalent quantity of electrical charge to enable the description of a meaningful electronics specification. Specifically, this quantity is dependent upon scintillating tile thickness, particle angle, light collection statistics, and PMT gain. The following parameters are assumed for this calculation.

5.1.8.1 PMT Gain

The nominal gain of the PMTs is 4×10^5 . This will be adjusted as required during the operation of the instrument by variation of the high voltage bias applied to the PMT.

5.1.8.2 Photoelectron Production

The nominal photoelectron production in the scintillating tiles is 20 photoelectrons per MIP. Two PMTs per tile will be utilized, providing a nominal 10 photoelectrons/MIP at the photocathode of each tube.

5.1.8.3 Photoelectron to Charge Conversion

The conversion to charge is $10 \text{ pe}^- \times 1.6022 \times 10^{-19} \text{ Coulombs} \times 4 \times 10^5 = 0.64 \text{ pC per MIP}$. The electronics will be designed and tested to this charge specification.

5.1.9 Signal Input Characteristics

The nominal signal source to the ACD electronics is supplied via a Hamamatsu R4443 PMT operating at the nominal gain specified above. The signal from the PMT will be AC-coupled from the anode via 340 pF

(two series 680 pF capacitors). The lower limit of the useful input signal range for singly charged particles will be 0.064 pC. The upper limit of the input signal range for singly charged particles will be 12.8 pC. The lower limit of the input signal range for heavy nuclei will be 6.4 pC. The upper limit of the input signal range for heavy nuclei will be 640 pC

5.1.10 Low Voltage Power

The low voltage power supplies used to supply the filtered +28V and regulated 3.3V to the ACD are located outside the ACD subsystem. The low voltage power supplies are required to have the following characteristics at the ACD interface connector in a bandwidth from 10 Hz to 10 MHz:

Supply	Min. (V)	Nom. (V)	Max. (V)	Min (mA)	Max (mA)	Max Ripple (mv RMS)
+3.3V	3.2	3.3	3.6	20	TBR	5
+28V	22.0	28.0	38.7*	20	TBR	10

*Expected to change to 28 +/- 1V

Low Voltage Power Supply Characteristics (Fig. X)

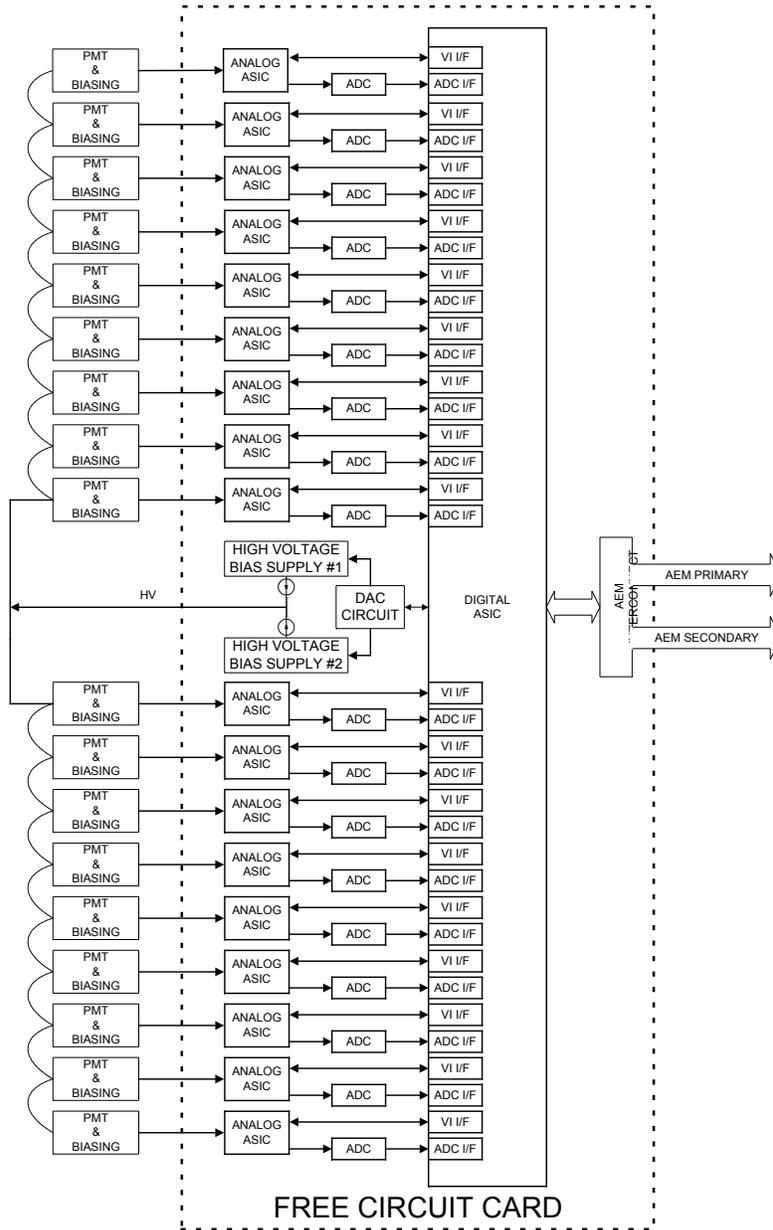
5.1.11 Thermistor Circuit

The ACD will use as temperature sensors YSI 44900 series 30K Ω thermistors, procured to the GSFC S-311P18 specification. These thermistors have an exponential temperature characteristic. The ACD will utilize these thermistors in measurements over the range of -40C to +60C

5.2 ACD Components

5.2.1 FRont-End Electronics

The FRont-End Electronics (FREE) provides the interface to the AEM for the front end ASICS and all the logic required for operation of these analog sections. Each individual ACD FREE circuit card can be represented in block diagram form as follows:



ACD FREE Circuit Card Block Diagram

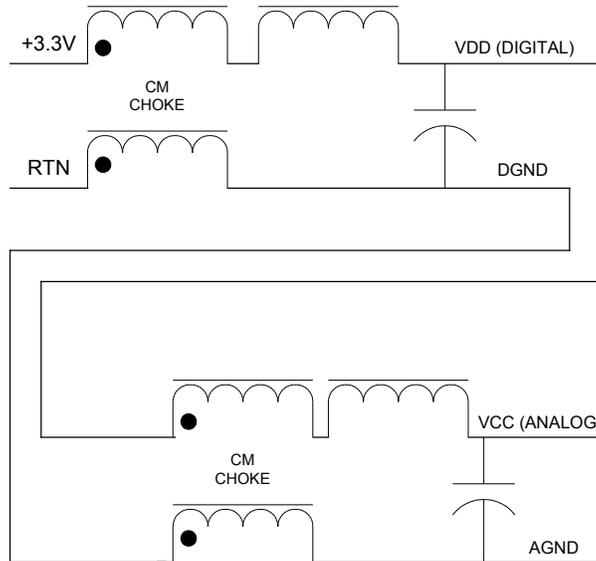
5.2.1.1 Output Requirements

Each FREE circuit card will produce the following outputs:

- ACD_NVETO_00 through ACD_NVETO_17 (VETO output for each channel)
- ACD_NCNO (logical OR of all enabled HLD on the FREE circuit card)
- ACD_NSDATA which is sent in response to L1T and contains 18 bits of VETO HitMap, 18 bits of PHA zero-suppression map, and up to 18 PHA words

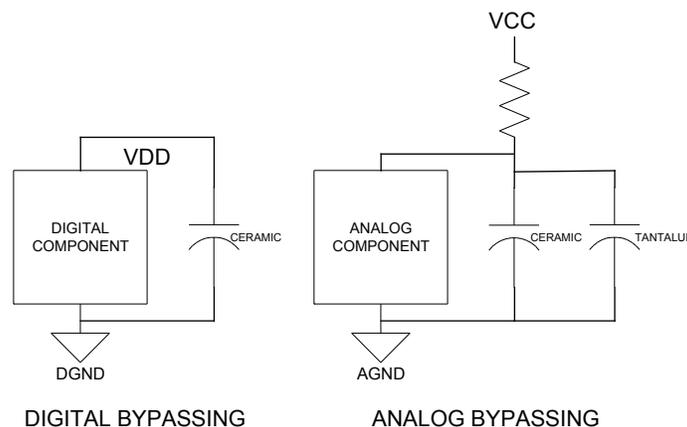
5.2.1.2 Power Filtering Circuitry

The FREE card will contain power-filtering circuitry in an attempt to limit the conducted susceptibility of the electronics. This filtering may consist of common-mode and single ended chokes, ceramic and tantalum capacitors, and series resistors. The proposed power filtering for the +3.3V power entering the board is detailed below.



The power filtering circuitry works in conjunction with the FREE grounding topology. All +3.3V current enters the board via the common mode choke and returns through the same path. The digital parts, such as GARC, are tied to the digital VDD power plane. The analog parts (such as GAFE, ADC, DAC, and the opamps) are tied to the VCC analog power plane, which is also isolated via a common mode choke. All analog current shall enter and return through the common mode choke.

Locally, the digital parts will be bypassed directly between the VDD and DGND planes with surface mounted ceramic capacitors. The analog parts will be bypassed through a resistor-capacitor network to the VCC and AGND planes. The nominal configuration for component bypassing is shown below.



The resistor for the analog bypass will be optimized for isolation versus voltage drop. All bypassing components will be placed close to their respective parts to maintain minimal sized power loops.

5.2.1.3 Digital Housekeeping

The ACD electronics will maintain a record of the last command received and a count of all valid commands and invalid commands received since power-on. The status of all ACD command registers will be transmitted to the AEM and telemetered at a low rate.

5.2.1.4 Analog Housekeeping

The LAT will monitor the ACD voltage rails to an accuracy of < 10 mV. The LAT will monitor the current used by each of the ACD low voltage rails to within 10 mA or 5%, whichever is smaller. The HVBSs associated with each FREE circuit card will produce an analog HV monitor voltage (0 to 2.5 volts), which will be transmitted to the LAT. The LAT will digitize the HV monitor signals to an accuracy of 0.4% and telemeter the results at a low rate (TBD). One temperature sensor shall be placed on each FREE circuit cards. The temperature sensor's analog output range is 0 to 2.5 volts and will be sensed by LAT electronics. The LAT will digitize the temperature signal from each FREE circuit card to an accuracy of 0.5°C or better, over a range of less than 80°C, and telemeter the results at a low rate (TBD).

5.2.1.5 Trigger Primitive Generation

There will be no trigger primitives generated by the ACD electronics.

5.2.1.6 Trigger Acknowledge (L1T) Signal

The AEM will transmit to each FREE circuit card the trigger command (L1T), which will cause the ACD ADC's to initiate conversion, the VETO Map (or the HLD Map in the appropriate test mode) to be latched, and those data to be prepared for transmission to the AEM. The L1T will be time-delayed to match the peaking time of the shaping amplifiers. The time delay shall be imposed by the GARC but programmed via command by the AEM.

5.2.1.7 Veto Hit Map Data

The ACD transmits the tile VETO hit map to the AEM, via the serial data interface, in response to L1T. This map indicates the occupancy of the ACD PMTs at the time of the event causing the L1T, ± 200 ns. Digital delay lines will be used to provide delays from 850 ns to 2400 ns with 50 nsec time steps. Digital pulse stretching up to 350 ns, in steps of 50 ns, will be provided to implement ± 200 nsec time coverage.

5.2.1.8 PHA Data

The ACD provides the PHA data to the AEM in response to a L1T. When requested by digital command, PHA data will be sent to the AEM via the serial data interface. There are commands that enable or disable each PHA, enable the readout of all PHA channels, and read out just the enabled PHA channels. There is no requirement for the minimum or maximum number of PHA words to be read out in Science mode for a science event.

5.2.1.9 Rate Counters - No Requirement

There is no requirement for rate counters in the ACD electronics. Rate counting will be performed by the AEM.

5.2.1.10 South Atlantic Anomaly Detection - No Requirement

There will be no method for detection of the SAA in the ACD electronics. The ACD electronics will not autonomously change (lower) the high voltage bias, even during high rate conditions. This function, as required by LAT-SS-00016 section 5.24, will be performed in the LAT data processing electronics.

5.2.1.11 Burst Processing

There are no requirements on the ACD electronics for the processing of either cosmic or solar transients. Any burst processing will be performed external to the ACD. The data rates that the ACD electronics will be tested to are as follows:

Data Type	Nominal Rate	Linear Rate Range	Maximum Rate
VETO, LLD	1000 Hz	3000 Hz	10,000 Hz
HLD	10 Hz	100 Hz	100 Hz
PHA	1000 Hz		10,000 Hz

5.2.1.12 Parts and PC Boards

Part Description	Source	Package
Resistors (thick film)	NPSL: MIL-PRF-55342	RM0705, RM1206
Ceramic Capacitors (100V)	NPSL: MIL-PRF-55681	CDR31, CDR32
Tantalum Capacitors	NPSL: MIL-PRF-55365	CWR09C-G
Analog ASIC	MOSIS	52-pin QFP (TBR)
Digital ASIC	MOSIS	208-pin QFP (TBR)
Analog-to-Digital Converters	Maxim MAX145	TBR
Digital-to-Analog Converters	MAX5121	TBR
Operational amplifiers	MAXIM 494	

5.2.1.13 PCB Fabrication

Flight PCBs will be fabricated to the IPC-6012 standard. Flight PCBs will be nominally either 0.062" or 0.093" thick and be constructed of either polyimide or FR-4. Flight PCBs will be assembled and inspected to NASA-STD-8739.3. After setup and functional testing, Flight PCBs will be conformal coated and staked with a Uralane 5750/5753 compound.

5.2.2 FREE Components

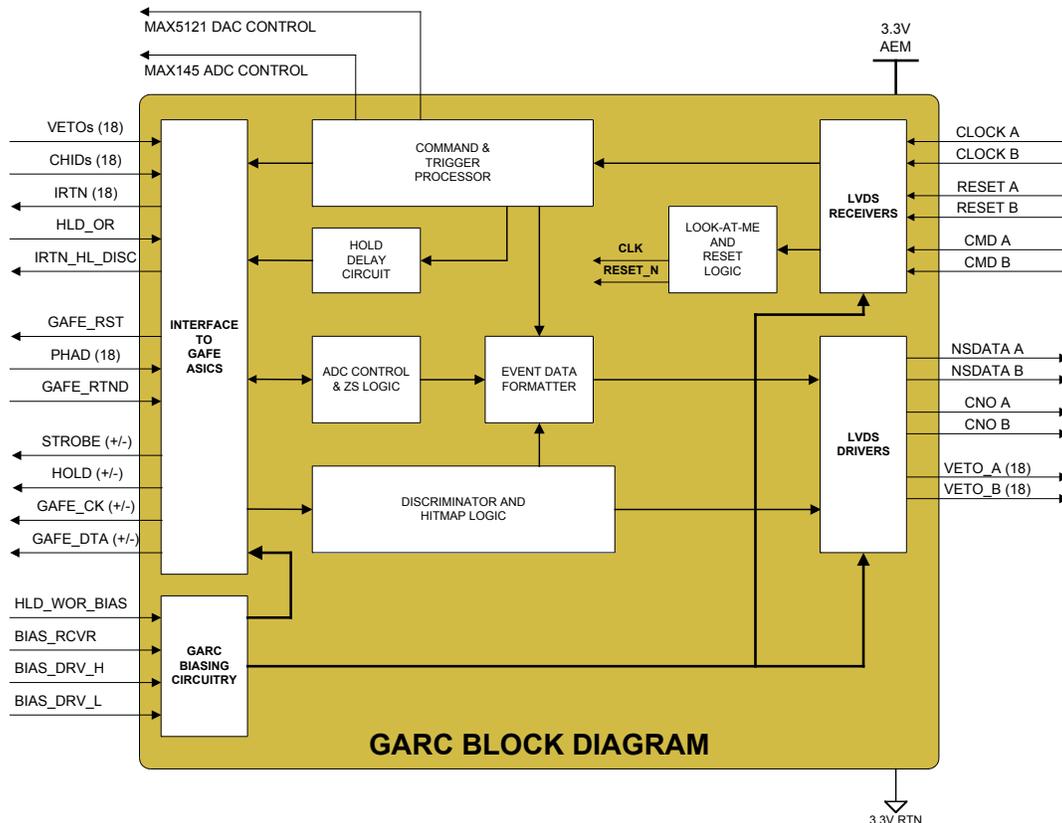
5.2.2.1 GLAST ACD Readout Controller ASIC (GARC)

The requirements for the GARC are derived from two sources: The GLAST ACD Electronics Level IV Requirements, LAT-SS-00352, and the GLAST ACD-AEM Interface Control Document, LAT-SS-00363. This section of the specifications document and describes the functionality of the GARC and how it meets these requirements.

One GARC is used on each FREE circuit card. It provides the interface between the eighteen (18) analog channels on the FREE circuit card and the LAT AEMs (primary and secondary). It provides for commandable configuration, triggering, and event data readout. The GARC also processes the GAFE VETO discriminators for transmission to the LAT. The GARC operates on a single 3.3V power supply. Digital interfaces to the AEM are custom-designed LVDS. Interfaces to the GAFE analog ASIC are custom current-mode drivers and receivers. The GARC die is packaged in a 208 pin plastic quad flatpack.

The GARC consists of a pad frame constructed of Tanner IO cells and spacers, custom-designed LVDS drivers and receivers for the AEM interface, custom-designed low current differential drivers and receivers for the GAFE interface, bias circuitry for these I/O cells, a clock distribution tree, a reset distribution tree, and the core logic module.

The core logic module is constructed of Tanner standard logic cells for the Agilent 0.5 um library and contains a command processor, an event data formatter, a discriminator logic module, an ADC control and zero-suppression logic module, a DAC controller, and logic to perform the primary vs. secondary switching and reset. A block diagram of the digital ASIC is shown below.



5.2.2.1.1 GARC Design Flow

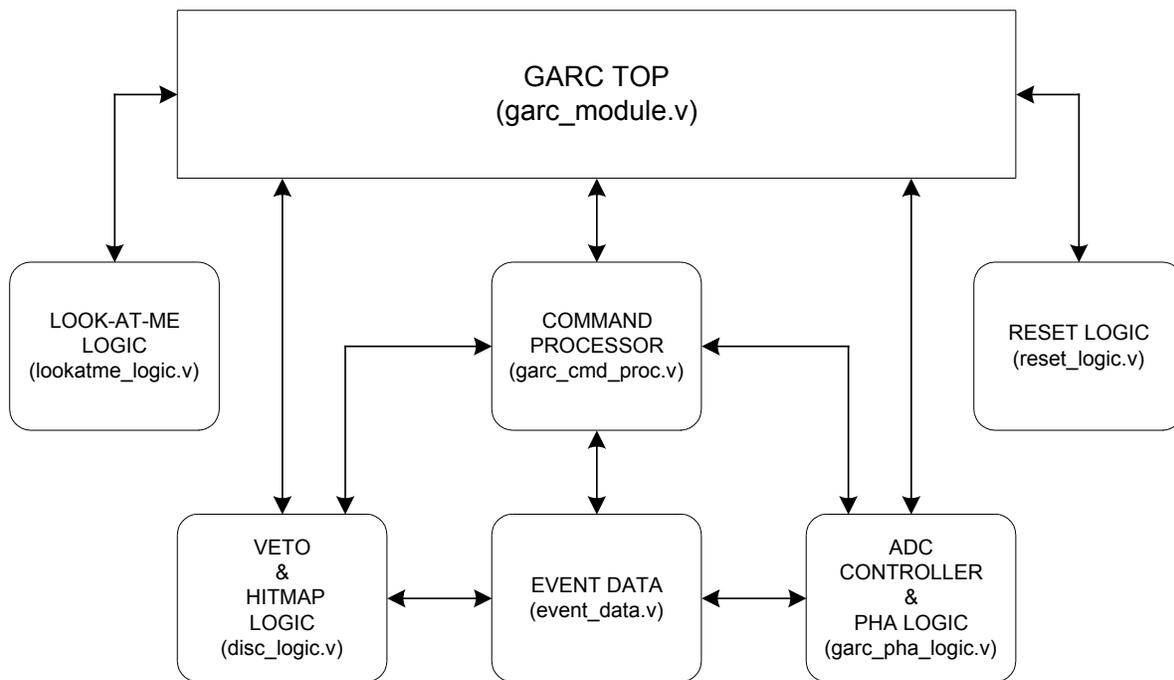
The GARC core logic is coded in Verilog. Simulation is performed via Cadence Verilog-XL. The ASIC design is also emulated in hardware via retargeting to an Altera FPGA.

The GARC uses the Mentor Graphics Exemplar Leonardo Spectrum synthesis tool to map the input Verilog files to the Agilent 0.5 μ m Tanner standard cell library. The output format of the Exemplar tool is EDIF.

The physical layout is performed using the Tanner L-Edit tool. The EDIF output from Exemplar is imported to L-Edit and then automatic cell placement and routing using three metal layers is performed using the Tanner SPR utility.

5.2.2.1.2 Hierarchy of the GARC Verilog Modules used in the Logic Core

The GARC Version 1 ASIC uses seven Verilog modules and has the following organizational structure.



**GARC LOGIC CORE HIERARCHY
(7 Verilog Modules)**

The top level module, **garc_module.v**, fixes the names of the I/O ports on the logic core and interconnects the signals for the six remaining logic modules. The command processor, **garc_cmd_proc.v**, is the largest logic module and handles all configuration and trigger read/write I/O. The event data module, **event_data.v**, is controlled by the command processor and formats the event data words. The VETO and HitMap logic module, **disc_logic.v**, handles the discriminator inputs from the GAFEs while the ADC controller handles the digitized pulse heights from the GAFE analog output. The ADC controller module, **garc_pha_logic.v**, controls the 18 analog-to-digital converters, stores and multiplexes the data, and provides the zero-suppression function. The look-at-me logic module, **lookatme_logic.v**, handles switching on the ACD side of the interface between primary and secondary

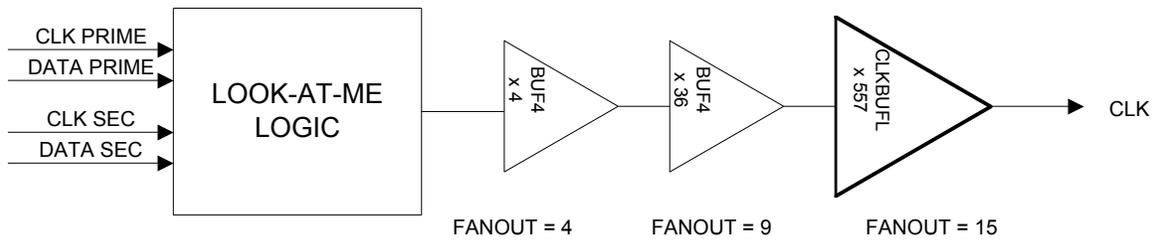
AEMs. The reset logic module, **reset_logic.v**, provides for a deglitched GARC reset to the logic core from either AEM command or power-on reset signals.

5.2.2.1.3 GARC Logic Clock Selection and Buffering Circuitry

The GARC clock is continuous and runs at a nominal 20 MHz. There are two paths for the clock to enter the GARC ASIC - one from the AEM Primary connector and one from the AEM Secondary connector. The Look-At-Me logic in the GARC selects the AEM side to view (power-on default is Primary) and routes this clock from the core to an external clock buffer. Each individual row of Tanner cells is also buffered again.

In the version 1 GARC, there are 60 rows of logic cells, each buffered by between 4 and 12 Tanner clock buffers (BufClkL). The clock from the Look-At-Me logic is buffered by four BUF4 cells, then again by another 36 BUF4 cells distributed evenly along the left edge of the core where the global clock rail is routed, and then finally by an additional 557 CLKBUFL cells along the 60 rows. All flip-flops not inside the Look-At-Me logic are clocked via the global CLK signal.

Pictorially, the CLK tree for GARC Version 1 is similar to the diagram below:



5.2.2.1.4 GARC Reset Circuitry

The GARC utilizes an active low global RESET_N signal to most of the Tanner flip-flops used in the logic core. The RESET_N is accomplished with the same topology as the clock tree, with the Look-At-Me logic driving 2 BUF4 drivers, then driving 574 RSTBUFR cells. Only the flip-flops in the Look-At-Me logic are not reset by the global RESET_N signal. The Tanner global reset trace is routed on the right side of the core module.

The GARC reset logic module requires that the RESET signal be present for a total of five consecutive clock cycles (i.e., 5 cycle deglitch) before allowing the reset to pass to the logic modules. Either the FREE circuit power-on reset or the AEM reset may reset the GARC logic.

5.2.2.1.5 Pin Description

The GARC has 208 I/O cells on the die for power, ground, and signal I/O. The Tanner standard pad library is used. The table below lists the five types of Tanner I/O pads and their utilization.

Tanner Pad Type	Pad Description	Pad Signal Type
PadVdd	Power Supply Pad	Vdd - Digital Power
PadGnd	Ground Pad	DGnd - Digital Ground
PadARef	Unbuffered Analog Pad	LVDS I/O, Discriminator Inputs, channel ID, GAFE IRTN, bias inputs
PadInC	Buffered Input Pad	CMOS Inputs

PadOut	Buffered Output Pad	CMOS Outputs
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The following is a list of the GARC Version 1 (May 2002) die pinout:

Tanner IO Cell	MOSIS Bond Pad Name	GARC Package Pin Number	GARC Signal Name
PADGnd	L1	1	DGND
PADAREF	L2	2	ACD_CLK_AP
PADAREF	L3	3	ACD_CLK_AM
PADAREF	L4	4	ACD_CLK_BP
PADAREF	L5	5	ACD_CLK_BM
PADAREF	L6	6	ACD_NSCMD_AP
PADAREF	L7	7	ACD_NSCMD_AM
PADAREF	K8	8	ACD_NSCMD_BP
PADAREF	L9	9	ACD_NSCMD_BM
PADAREF	L10	10	ACD_NRST_AP
PADAREF	L11	11	ACD_NRST_AM
PADAREF	L12	12	ACD_NRST_BP
PADAREF	L13	13	ACD_NRST_BM
PADAREF	L14	14	ACD_NSDATA_AP
PADAREF	L15	15	ACD_NSDATA_AM
PADAREF	L16	16	ACD_NSDATA_BP
PADAREF	L17	17	ACD_NSDATA_BM
PADAREF	L18	18	ACD_NCNO_AP
PADAREF	L19	19	ACD_NCNO_AM
PADAREF	L20	20	ACD_NCNO_BP
PADAREF	L21	21	ACD_NCNO_BM
PADAREF	L22	22	ACD_NVETO_00AP
PADAREF	L23	23	ACD_NVETO_00AM
PADVdd	L24	24	DVDD
PADAREF	L25	25	ACD_NVETO_00BP
PADAREF	L26	26	ACD_NVETO_00BM
PADGnd	L27	27	DGND
PADAREF	L28	28	ACD_NVETO_01AP
PADAREF	L29	29	ACD_NVETO_01AM
PADAREF	L30	30	ACD_NVETO_01BP
PADAREF	L31	31	ACD_NVETO_01BM
PADAREF	L32	32	ACD_NVETO_02AP
PADAREF	L33	33	ACD_NVETO_02AM
PADAREF	L34	34	ACD_NVETO_02BP
PADAREF	L35	35	ACD_NVETO_02BM
PADAREF	L36	36	ACD_NVETO_03AP
PADAREF	L37	37	ACD_NVETO_03AM
PADAREF	L38	38	ACD_NVETO_03BP
PADAREF	L39	39	ACD_NVETO_03BM
PADAREF	L40	40	ACD_NVETO_04AP
PADAREF	L41	41	ACD_NVETO_04AM
PADAREF	L42	42	ACD_NVETO_04BP
PADAREF	L43	43	ACD_NVETO_04BM
PADAREF	L44	44	ACD_NVETO_05AP
PADAREF	L45	45	ACD_NVETO_05AM
PADAREF	L46	46	ACD_NVETO_05BP
PADAREF	L47	47	ACD_NVETO_05BM

PADAREF	L48	48	ACD_NVETO_06AP
PADAREF	L49	49	ACD_NVETO_06AM
PADAREF	L50	50	ACD_NVETO_06BP
PADAREF	L51	51	ACD_NVETO_06BM
PADVdd	L52	52	DVDD
PADGnd	B1	53	DGND
PADAREF	B2	54	ACD_NVETO_07AP
PADAREF	B3	55	ACD_NVETO_07AM
PADAREF	B4	56	ACD_NVETO_07BP
PADAREF	B5	57	ACD_NVETO_07BM
PADAREF	B6	58	ACD_NVETO_08AP
PADAREF	B7	59	ACD_NVETO_08AM
PADAREF	B8	60	ACD_NVETO_08BP
PADAREF	B9	61	ACD_NVETO_08BM
PADAREF	B10	62	ACD_NVETO_09AP
PADAREF	B11	63	ACD_NVETO_09AM
PADAREF	B12	64	ACD_NVETO_09BP
PADAREF	B13	65	ACD_NVETO_09BM
PADAREF	B14	66	ACD_NVETO_10AP
PADAREF	B15	67	ACD_NVETO_10AM
PADAREF	B16	68	ACD_NVETO_10BP
PADAREF	B17	69	ACD_NVETO_10BM
PADAREF	B18	70	ACD_NVETO_11AP
PADAREF	B19	71	ACD_NVETO_11AM
PADAREF	B20	72	ACD_NVETO_11BP
PADAREF	B21	73	ACD_NVETO_11BM
PADAREF	B22	74	ACD_NVETO_12AP
PADAREF	B23	75	ACD_NVETO_12AM
PADAREF	B24	76	ACD_NVETO_12BP
PADAREF	B25	77	ACD_NVETO_12BM
PADVdd	B26	78	DVDD
PADAREF	B27	79	CHID_17
PADGnd	B28	80	DGND
PADAREF	B29	81	DISC_17
PADAREF	B30	82	IRTN_17
PADAREF	B31	83	CHID_16
PADAREF	B32	84	DISC_16
PADAREF	B33	85	IRTN_16
PADAREF	B34	86	CHID_15
PADAREF	B35	87	DISC_15
PADAREF	B36	88	IRTN_15
PADAREF	B37	89	CHID_14
PADAREF	B38	90	DISC_14
PADAREF	B39	91	IRTN_14
PADAREF	B40	92	CHID_13
PADAREF	B41	93	DISC_13
PADAREF	B42	94	IRTN_13
PADAREF	B43	95	CHID_12
PADAREF	B44	96	DISC_12
PADAREF	B45	97	IRTN_12
PADAREF	B46	98	CHID_11
PADAREF	B47	99	DISC_11
PADAREF	B48	100	IRTN_11

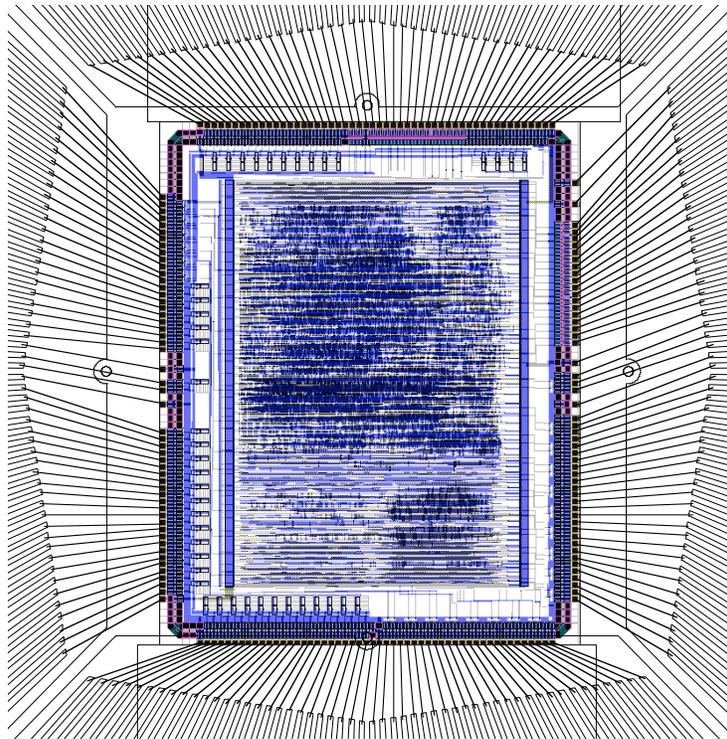
PADAREF	B49	101	CHID_10
PADAREF	B50	102	DISC_10
PADAREF	B51	103	IRTN_10
PADAREF	B52	104	HLD_WOR_BIAS
PADAREF	R52	105	CHID_09
PADAREF	R51	106	DISC_09
PADAREF	R50	107	IRTN_09
PADAREF	R49	108	CHID_08
PADAREF	R48	109	DISC_08
PADAREF	R47	110	IRTN_08
PADAREF	R46	111	CHID_07
PADAREF	R45	112	DISC_07
PADAREF	R44	113	IRTN_07
PADAREF	R43	114	CHID_06
PADAREF	R42	115	DISC_06
PADAREF	R41	116	IRTN_06
PADAREF	R40	117	CHID_05
PADAREF	R39	118	DISC_05
PADAREF	R38	119	IRTN_05
PADAREF	R37	120	CHID_04
PADAREF	R36	121	DISC_04
PADAREF	R35	122	IRTN_04
PADAREF	R34	123	CHID_03
PADAREF	R33	124	DISC_03
PADAREF	R32	125	IRTN_03
PADAREF	R31	126	CHID_02
PADAREF	R30	127	DISC_02
PADAREF	R29	128	IRTN_02
PADAREF	R28	129	CHID_01
PADAREF	R27	130	DISC_01
PADAREF	R26	131	IRTN_01
PADVdd	R25	132	DVDD
PADAREF	R24	133	CHID_00
PADAREF	R23	134	DISC_00
PADAREF	R22	135	IRTN_00
PADGnd	R21	136	DGND
PADInC	R20	137	PHAD_17
PADInC	R19	138	PHAD_16
PADInC	R18	139	PHAD_15
PADInC	R17	140	PHAD_14
PADInC	R16	141	PHAD_13
PADInC	R15	142	PHAD_12
PADInC	R14	143	PHAD_11
PADInC	R13	144	PHAD_10
PADInC	R12	145	PHAD_09
PADInC	R11	146	PHAD_08
PADInC	R10	147	PHAD_07
PADInC	R9	148	PHAD_06
PADInC	R8	149	PHAD_05
PADInC	R7	150	PHAD_04
PADInC	R6	151	PHAD_03
PADInC	R5	152	PHAD_02
PADInC	R4	153	PHAD_01

PADInC	R3	154	PHAD_00
PADVdd	R2	155	DVDD
PADAREF	R1	156	BIAS_RCVR
PADGnd	T52	157	DGND
PADAREF	T51	158	IRTN_HL_DISC
PADAREF	T50	159	OR_HL_DISC
PADAREF	T49	160	BIAS_DRV_H
PADAREF	T48	161	GAFE_HOLDP
PADAREF	T47	162	GAFE_HOLDM
PADAREF	T46	163	GAFE_STROBEP
PADAREF	T45	164	GAFE_STROBEM
PADAREF	T44	165	GAFE_DATP
PADAREF	T43	166	GAFE_DATM
PADAREF	T42	167	GAFE_CLKP
PADAREF	T41	168	GAFE_CLKM
PADAREF	T40	169	BIAS_DRV_L
PADInC	T39	170	GAFE_RET_DATA
PadOut	T38	171	GAFE_RST
PADOut	T37	172	ADC_CLK
PADOut	T36	173	NADC_CS
PADOut	T35	174	DAC_CLK
PADOut	T34	175	DAC_DATA
PADInC	T33	176	DAC_READBACK
PADOut	T32	177	NDAC_CS
PADOut	T31	178	NDAC_CLR
PADOut	T30	179	HITMAP_TEST
PADOut	T29	180	TRIG_TST
PADInC	T28	181	FREE_ID
PADInC	T27	182	PWR_ON_RST
PADOut	T26	183	VETO_ENA_TST
PADAREF	T25	184	LVDS_PRESETADJ
PADOut	T24	185	HV_ENABLE_1
PADOut	T23	186	HV_ENABLE_2
PADGnd	T22	187	DGND
PADAREF	T21	188	ACD_NVETO_17AP
PADAREF	T20	189	ACD_NVETO_17AM
PADAREF	T19	190	ACD_NVETO_17BP
PADAREF	T18	191	ACD_NVETO_17BM
PADAREF	T17	192	ACD_NVETO_16AP
PADAREF	T16	193	ACD_NVETO_16AM
PADAREF	T15	194	ACD_NVETO_16BP
PADAREF	T14	195	ACD_NVETO_16BM
PADAREF	T13	196	ACD_NVETO_15AP
PADAREF	T12	197	ACD_NVETO_15AM
PADAREF	T11	198	ACD_NVETO_15BP
PADAREF	T10	199	ACD_NVETO_15BM
PADAREF	T9	200	ACD_NVETO_14AP
PADAREF	T8	201	ACD_NVETO_14AM
PADAREF	T7	202	ACD_NVETO_14BP
PADAREF	T6	203	ACD_NVETO_14BM
PADAREF	T5	204	ACD_NVETO_13AP
PADAREF	T4	205	ACD_NVETO_13AM
PADAREF	T3	206	ACD_NVETO_13BP

PADAREF	T2	207	ACD_NVETO_13BM
PADVdd	T1	208	DVDD

5.2.2.1.7 GARC Die Packaging

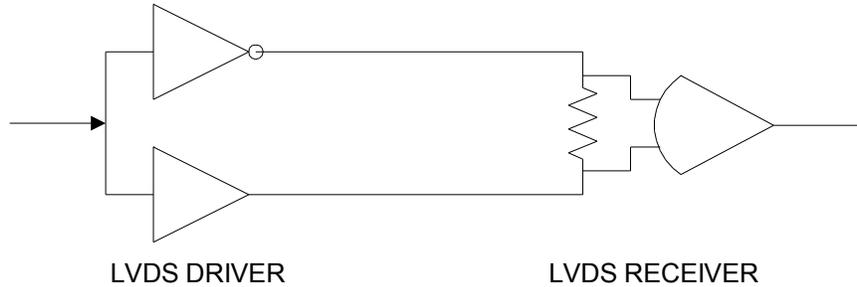
The GARC is packaged in a 208 pin 28.0 mm x 28.0 mm plastic quad flatpack (ASAT QFP208B) with leads on a 0.5 mm pitch. This package is available through MOSIS through ASAT. (<http://www.asat.com/products/leaded/tqfp.htm>). The bonding diagram is shown below (die is not to scale in relation to lead frame).



GARC BONDING DIAGRAM

5.2.2.1.8 LVDS Drivers and Receivers for GARC to AEM Communication

The FREE circuit cards utilize the digital ASICs as a means of communicating with the AEM. The digital communications protocol is standard LVDS, utilizing a 3.5 mA current. A functional diagram of the interface is shown below.



The value of the termination resistor is 100 Ω . The voltage levels at the input and outputs are 0V and 3.3V. In the GARC, there are 40 LVDS drivers (ACD_NSDATA, ACD_CNO, ACD_VETO) and 6 LVDS receivers (ACD_CLK, ACD_NSCMD, ACD_NRST). The nominal bias setting is controlled externally via bias resistors. The maximum switch rate utilized in the GARC is 20 MHz.

5.2.2.1.9 Analog I/O Modules for GARC to GAFE Communication

The GARC has 64 I/O signals for communication with the 18 GAFE ASICs. These consist of four differential control signals (HOLD, STROBE, DATA, CLK), 18 channel identification inputs, 19 discriminator inputs (18 VETO + 1 HLD), and 19 driver current returns (IRTN). These I/O modules are custom-designed to interface with the corresponding cells in the GAFE. Since these signals are for ASIC to ASIC communication on the same board, they utilize an order of magnitude less drive current than the LVDS standard used between the GARC and AEM.

5.2.2.1.10 Nominal Bias Resistor Settings

There are several external bias resistors required by the GARC. A table of these signals and the nominal values is included below.

GARC Bias Signal	GARC Pin	Nominal Bias Resistor Required	Function of Bias Resistor
HLD_WOR_BIAS	104	7 k Ω to DGND	HLD Wired-OR Rcvr Bias
BIAS_RCVR	156	84 k Ω to VDD	LVDS Rcvr Bias Adjust
BIAS_DRV_H	160	7 k Ω to DGND	LVDS Driver Bias Adjust
BIAS_DRV_L	169	7 k Ω to DGND	LLDRV Driver Bias Adjust
LVDS_PRESETADJ	184	7 k Ω to VDD	LVDS Preset Adjust

5.2.2.1.11 GARC Look-At-Me Circuitry

The GARC is connected to a clock (ACD_CLK) and command data (ACD_NSCMD) for both the Primary AEM side and the Secondary AEM side. Only one AEM is supposed to be active at a time and the GARC needs a mechanism to be able to dynamically switch the command receiver dependent upon which AEM is active. The Look-At-Me circuitry performs this function.

To switch the GARC to the active AEM side, the AEM sends a unique look-at-me command, 34'h24153D721, to the GARC. The GARC recognizes this command, performs the multiplexer switch, and provides readback in the GARC Status register. The power-on default for GARC is the Primary side.

5.2.2.1.12 Processing the VETO_AEM and HitMap Signals

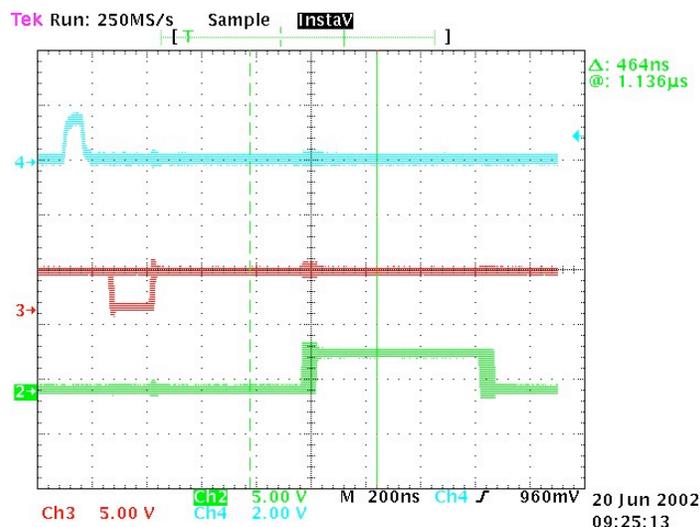
The GARC receives VETO discriminator inputs from up to eighteen (18) GAFE ASICs mounted on the FREE card. Each of the discriminators input to the GARC is active high and indicative of the duration in time that the charge input exceeds a preset threshold in the GAFE. The GARC contains circuitry to delay and deglitch these inputs to construct the VETO_AEM outputs, the VETO signals transmitted to the AEM.

A commandable delay tap is input to a deglitch circuit that requires the delayed comparator signal to be present for a minimum of two consecutive clock cycles prior to admitting the pulse. Once the pulse is detected, a retriggerable, programmable digital one-shot is initiated. The delay from the discriminator input to the output of the pulse and the width of the output pulse are commandable.

The discriminator inputs from the GAFE are also used to generate the VETO HitMap, an eighteen bit word that is returned as part of the event data transmission. This event data occurs in response to an AEM trigger request. This HitMap word captures the state of the input discriminators at a preset time in relation to the receipt of the trigger command from the AEM. The delay from discriminator input to HitMap latch, the minimum pulse width of the HitMap signal, and the deadtime added to the trailing edge of the HitMap pulse are all commandable. The pulse is sampled at a unique point in the readout cycle, the start of the analog-to-digital conversion. This signal is not deglitched.

The GARC version 1 logic has been emulated utilizing an Altera FPGA. The GARC core has been retargeted to Altera cells and integrated with a simulated AEM and simulated GAFEs. Test signals have been mapped to pins on the Altera for functional verification. The Altera test board has been run with a 20 MHz clock. Many of the I/O signals have been captured on the oscilloscope and plotted below.

The operation of the VETO deglitching circuit and the HitMap circuit is shown in the scope plot below. Channel 1 is the discriminator input, channel 2 is the VETO output, and channel 3 is the HitMap test point. In this case, the input discriminator width is set to the point where the VETO pulse is present approximately 50% of the time, which corresponds to a discriminator input of approximately 100 ns. The oscilloscope was set to a persistence of 500 msec to show this feature more clearly. Note that there is not a similar effect for the HitMap since it is not deglitched.



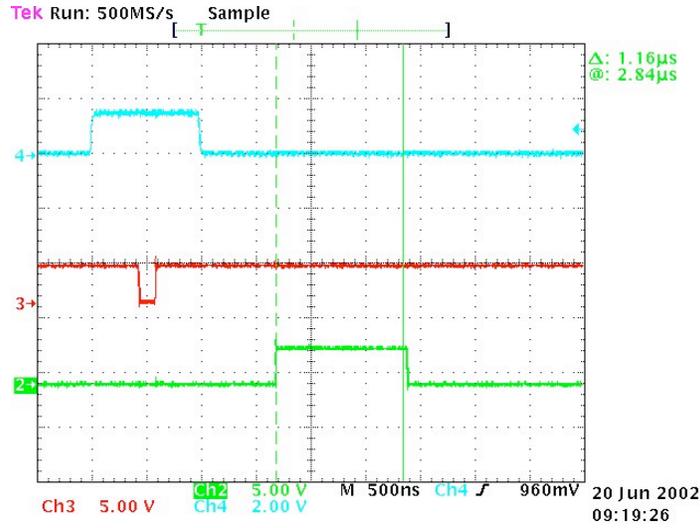
GARC Version 1 has the following commandable adjustments to the VETO and HitMap timing:

Commandable Parameter	Adjustment Range	Default Value	Adjustment Step
VETO Delay	150 to 1700 ns	400 ns	50 ns
VETO Width	50 to 400 ns	150 ns	50 ns
HitMap Delay	850 to 2400 ns	500 ns	50 ns
HitMap Width	150 to 900 ns	150 ns	50 ns

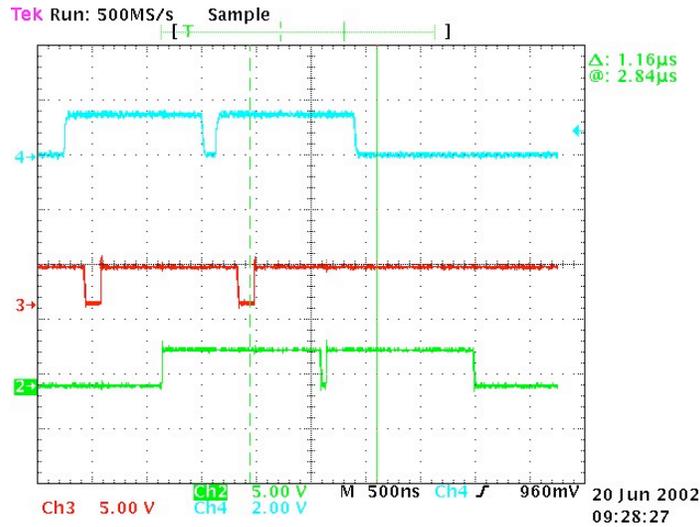
HitMap Deadtime	0 to 350 ns	1650 ns	50 ns
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The GARC also has 18 bits for the enable or disable of VETO signals. By default, all VETO signals are enabled but this capability exists so that individual discriminator channels may be digitally turned off.

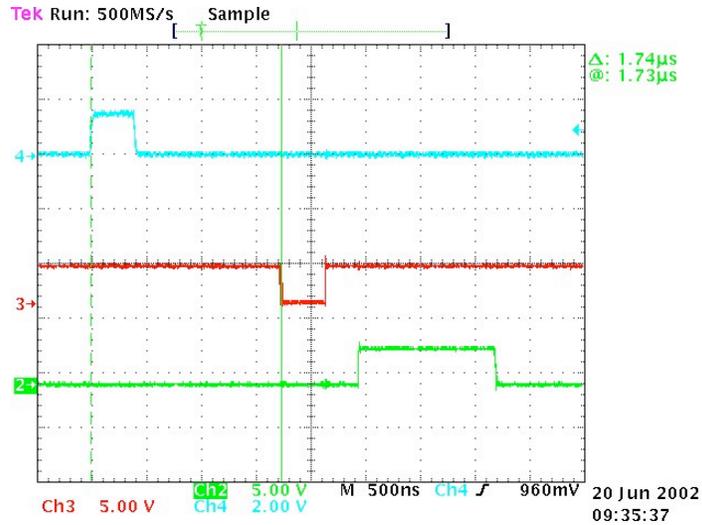
The nominal timing of the VETO and HitMap pulses at the default settings is shown below. Channel 4 (top) is the pulse used as the Discriminator Input (simulating the GAFE discriminator). Channel 3 (middle trace) is the AEM_VETO pulse. Channel 2 (bottom trace) is the HitMap test point. In the plot below, the discriminator input width is 1000 ns. The Veto_Delay = 450 ns and the Veto_Width = 150 ns. The HitMap_Delay = 1700 ns and the HitMap_Width = 1150 ns.



For pulses close together, the VETO circuit works as shown below.



At the maximum VETO and HitMap delays (e.g., VETO_Delay = 31 = 1700 ns, VETO_Width = 7 = 400 ns, HitMap_Delay = 31 = 1650 ns, HitMap_Width = 15 = 900 ns, HitMap_Deadtime = 7 = 300ns), we see the following timing:



The specific details, requirements, and a diagram of the VETO_AEM timing are contained in the ACD-AEM ICD, LAT-SS-00363.

5.2.2.1.13 GARC Command Processor

The command processing state machine (`garc_cmd_proc.v`) is utilized by the digital ASIC for configuration and readback of registers contained within the GARC. There are three types of commands – configuration commands (GARC or GAFE), readback commands (GARC or GAFE), and trigger commands (zero-suppressed or non zero-suppressed). All registers in either the GARC or GAFE may be read via readback command. Some registers in GARC and GAFE are read-only registers and do not have a corresponding write command (e.g., diagnostic and status registers). All GARC and GAFE registers are initialized to predetermined values upon RESET. The definitions of the GARC and GAFE registers accessible by digital command is contained in the ACD-AEM ICD, LAT-SS-00363.

Commands are sent serially from the AEM to the digital ASIC via a clock and data interface. The GARC command processor waits for a command to start filling the command shift register. After four bits are in the command shift register, the state machine checks if these four bits represent a trigger command. If the command is a valid trigger, then a trigger is executed.

If a trigger command is not contained in the first four bits, then the command processor waits for a 34-bit word to fill the shift register. At this point, the shift register is inhibited from filling. The parity for the entire command word is checked. If it is correct, then the command is decoded. If it is incorrect, then the command is rejected and information related to the error is loaded into GARC diagnostic registers. Commands with proper parity but with unassigned address codes are executed as no-operations. Command parity is odd and consists of three bits – one covering the command address and function and one covering the data bits.

The command format for the four bit trigger commands is as follows:



and the command format for the 34 bit configuration commands is as follows:

1	0	0	1	n	aaaaa	m	1	rrrr	p	dddd	p
33	32	31	30	29	28:24	23	22	21:18	17	16:1	0

Bit 29 - 0 for GARC, 1 for GAFE

Bits 28:24 - Address/Function Select

Bit 23 - 0 for Write, 1 for Read

Bits 21:18 - Register Select

Bit 17 - Odd parity over previous 15 bits

Bits 16:1 - Command Data

Bit 0 - Odd parity over Command Data

CONFIGURATION COMMAND FORMAT

The readback format for GARC register configuration is:

1	S	aaaaa	m	1	rrrr	p	dddd	e	p
31	30	29:25	24	23	22:19	18	17:2	1	0

Bit 30 - 0 for GARC, 1 for GAFE

Bits 29:25 - Address/Function Select

Bit 24 - Always 1 for Read

Bits 21:18 - Register Select

Bit 18 - Odd parity over previous 12 bits

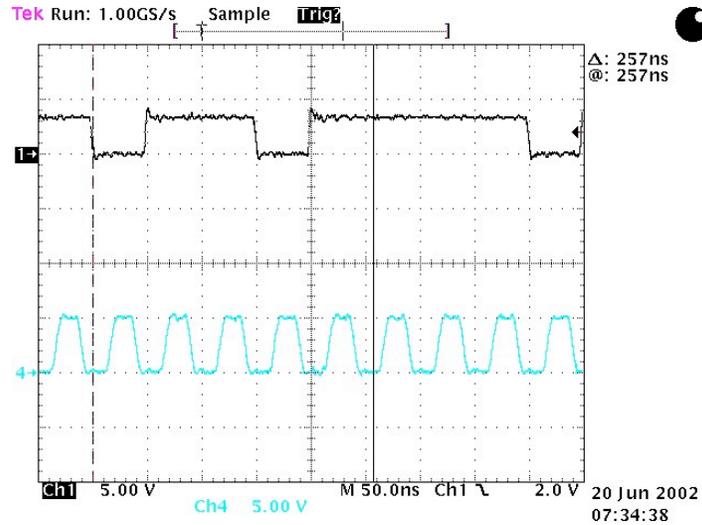
Bits 17:2 - Data, MSB First

Bit 1 - Error in parity detected

Bit 0 - Odd parity over previous 17 bits

CONFIGURATION READBACK FORMAT

The phasing of the GARC command and data is as shown below, with the command data shifting out of the AEM on the falling edge of the clock, latched into the GARC on the rising edge of the clock.



A table of registers available in the GARC Version 1 (May 2002) and in each GAFE is given below.

GARC or GAFE	Function Block and/or Register Address	Register Name	Register Bits	Initial Value upon Reset
GAFE	0	CONFIG_REG	16	16'h0030 = 48
GAFE	1	VETO_DAC	6	57
GAFE	2	HLD_DAC	6	38
GAFE	3	LLD_DAC	6	55
GAFE	4	BIAS_DAC	6	32
GAFE	5	TCI_DAC	6	0
GAFE	6	VERS_ADDR	6	2
GAFE	7	WRITE_CTR	6	0
GAFE	8	REJECT_CTR	6	0
GAFE	10	CHIP_ADDR	5	Hard Wired Addr
GARC	FB = 0, RA = 2	Veto_Delay	5	5
GARC	FB = 0, RA = 8	HVBS Level	12	0
GARC	FB = 0, RA = 9	SAA Level	12	0
GARC	FB = 0, RA = 12	Hold Delay	7	28
GARC	FB = 0, RA = 13	Veto Width	3	2
GARC	FB = 0, RA = 14	HitMap Width	4	7
GARC	FB = 0, RA = 15	HitMap Deadtime	3	3
GARC	FB = 1, RA = 8	HitMap Delay	5	16
GARC	FB = 1, RA = 9	PHA EN0 Register	16	65535
GARC	FB = 1, RA = 10	Veto EN0 Register	16	65535
GARC	FB = 1, RA = 11	HLD EN0 Register	16	65535
GARC	FB = 1, RA = 12	PHA EN1 Register	2	3
GARC	FB = 1, RA = 13	Veto EN1 Register	2	3
GARC	FB = 1, RA = 14	HLD EN1 Register	2	3
GARC	FB = 1, RA = 15	Max PHA	5	4
GARC	FB = 2, RA = 8	GARC Mode	11	768
GARC	FB = 2, RA = 9	GARC Status	6	24
GARC	FB = 2, RA = 10	Command Register	16	0
GARC	FB = 2, RA = 12	Command Rejects	8	0

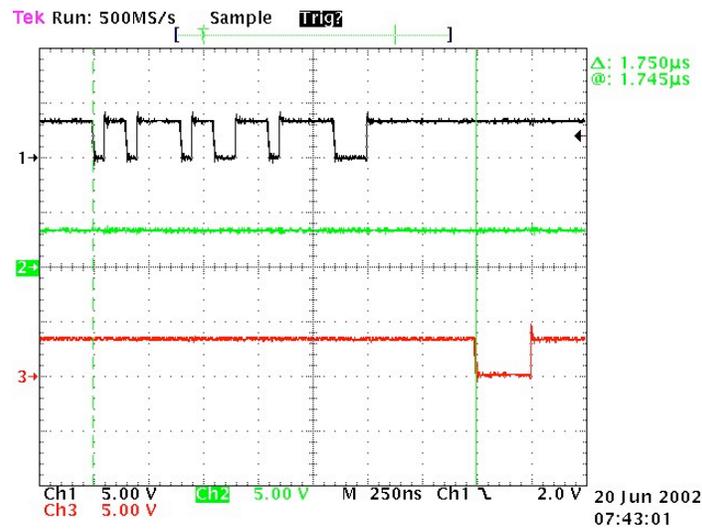
GARC	FB = 2, RA = 13	FREE Board ID	8	< 255
GARC	FB = 2, RA = 14	GARC Version	3	1
GARC	FB = 3, RA = 8	PHA Threshold 0	12	1114
GARC	FB = 3, RA = 9	PHA Threshold 1	12	1114
GARC	FB = 3, RA = 10	PHA Threshold 2	12	1114
GARC	FB = 3, RA = 11	PHA Threshold 3	12	1114
GARC	FB = 3, RA = 12	PHA Threshold 4	12	1114
GARC	FB = 3, RA = 13	PHA Threshold 5	12	1114
GARC	FB = 3, RA = 14	PHA Threshold 6	12	1114
GARC	FB = 4, RA = 8	PHA Threshold 7	12	1114
GARC	FB = 4, RA = 9	PHA Threshold 8	12	1114
GARC	FB = 4, RA = 10	PHA Threshold 9	12	1114
GARC	FB = 4, RA = 11	PHA Threshold 10	12	1114
GARC	FB = 4, RA = 12	PHA Threshold 11	12	1114
GARC	FB = 4, RA = 13	PHA Threshold 12	12	1114
GARC	FB = 4, RA = 14	PHA Threshold 13	12	1114
GARC	FB = 5, RA = 8	PHA Threshold 14	12	1114
GARC	FB = 5, RA = 9	PHA Threshold 15	12	1114
GARC	FB = 5, RA = 10	PHA Threshold 16	12	1114
GARC	FB = 5, RA = 11	PHA Threshold 17	12	1114
GARC	FB = 5, RA = 12	ADC TACQ	6	0

The measured configuration command processing times (at the nominal 20 MHz clock) for GARC Version 1 (May 2002) are as follows:

Configuration Command Type	Processing time in nanoseconds
All GARC Write Configuration except as below	2000
All GARC Read Configuration except as below	3550
Cal Pulse	2000
Reset	2000
Set HVBS DAC	5400
Read HVBS DAC	7100
GAFE Configuration Write	12250
GAFE Configuration Read	13900

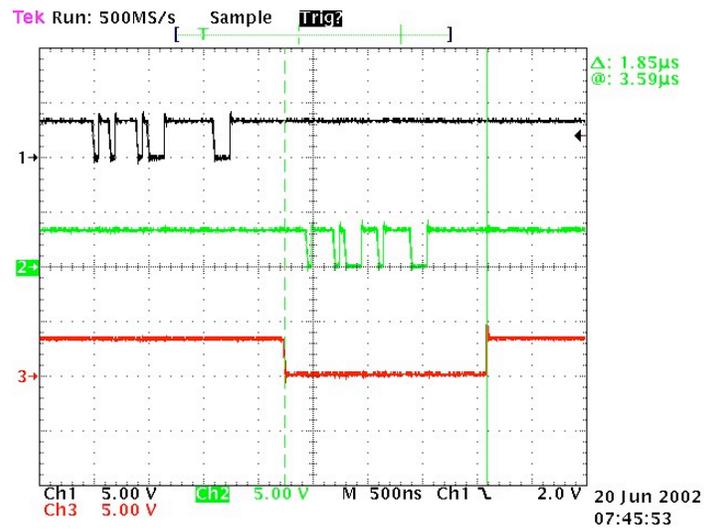
The processing times for GARC Version 1 trigger commands can be calculated as shown in the ICD.

The timing for a GARC configuration register write command is shown below.



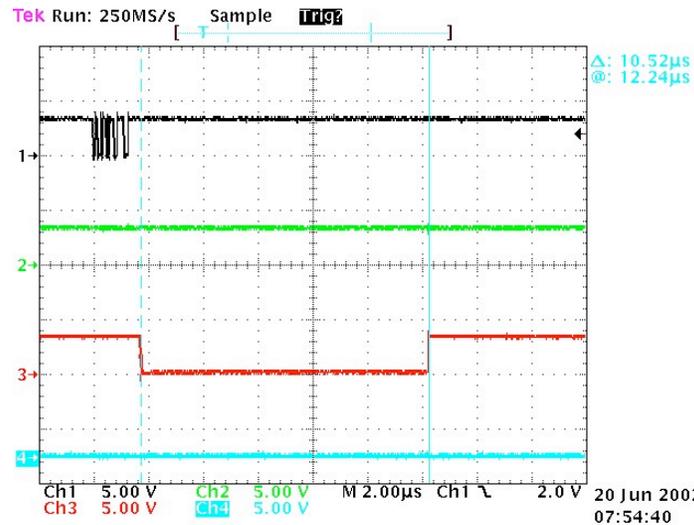
Channel 1 is the command data from the AEM. Channel 2 is the configuration readback data. Channel 3 is the state machine Live time (active high represents Live). The scope trace shows a command processing time of 250 ns.

The timing for a GARC configuration register read command is shown below.



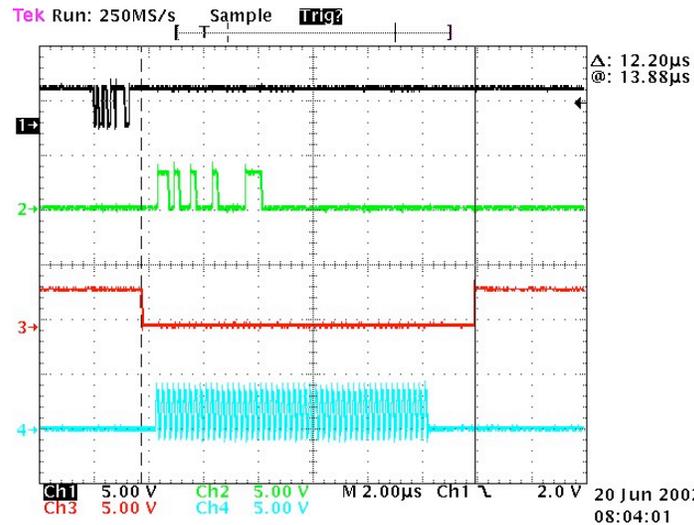
Channel 1 is the command data from the AEM. Channel 2 is the configuration readback data. Channel 3 is the state machine Live time (active high represents Live). The scope trace shows a readback command processing time of approximately 1850 ns.

The timing for a command written to one of the GAFE ASICs is shown below.



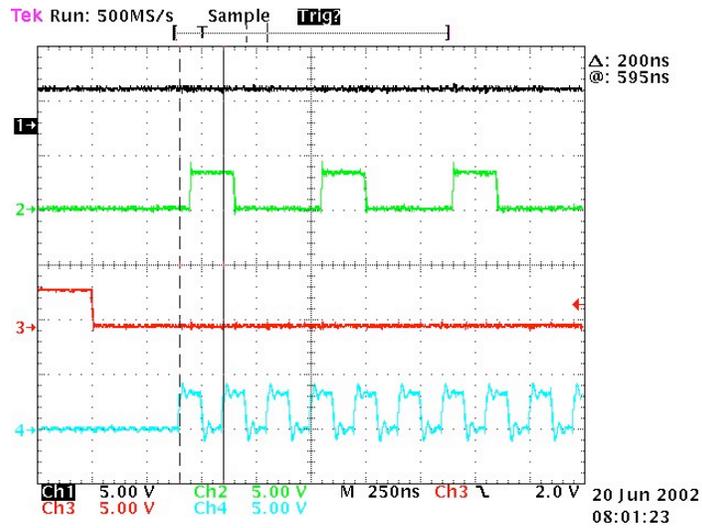
Channel 1 is GARC command data. Channel 2 is GARC return data. Channel 3 is GARC command processor Live time, shown to be inactive for approximately 10500 ns in this plot. GAFE commands are written at 5 MHz.

The timing for a configuration readback command from one of the GAFE ASICs is shown below.



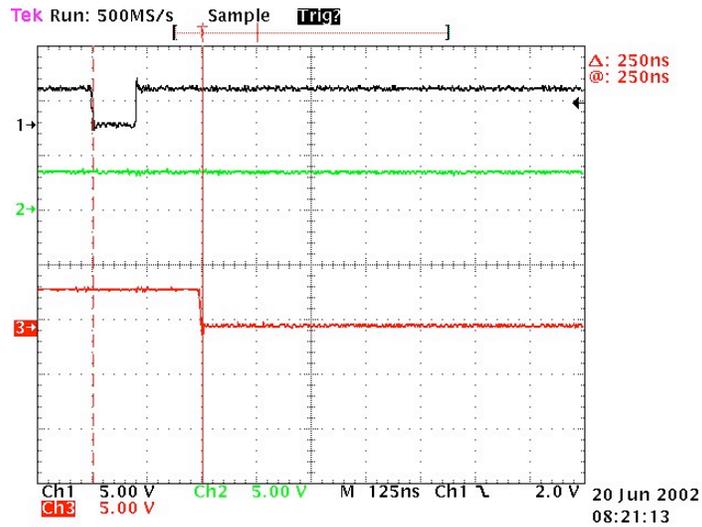
Channel 1 is GARC command data. Channel 2 is GAFE command data. Channel 3 is GARC command processor Live time, measured in the plot at approximately 12200 ns. Channel 4 is the GAFE command clock.

A closer view of the GAFE command data and GAFE command clock phasing is shown below.

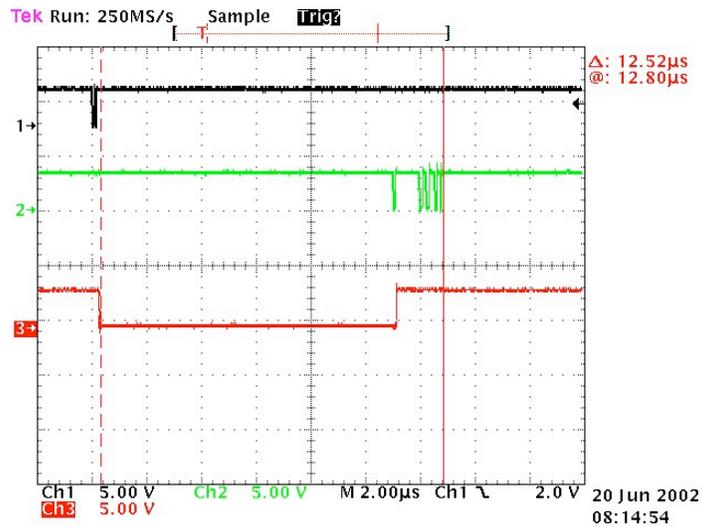


The GAFE command clock period is derived from the GARC 20 MHz clock and is nominally 200 ns. This clock is only active during a GAFE command and is at 0V at all other times.

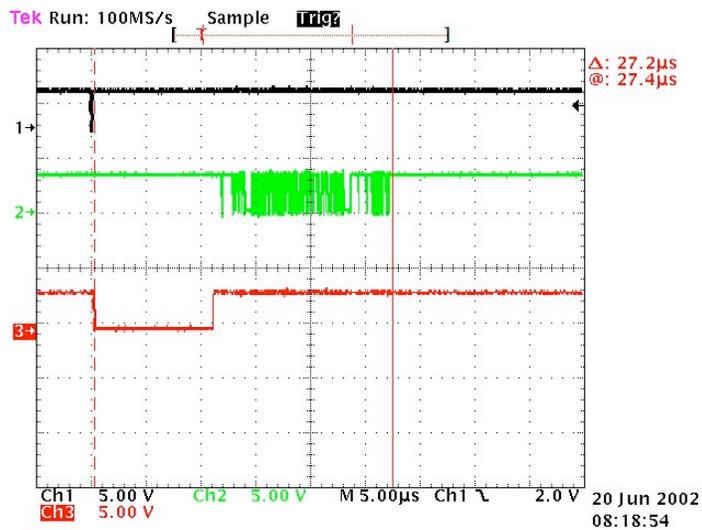
The following plot shows the execution of the zero-suppressed trigger command (e.g., 1100). There is a delay of 250 ns from the leading edge of the first command bit until the trigger is active.



The minimum time duration for processing of a trigger command (default settings) with no PHA returned is shown below (approximately 12500 ns)



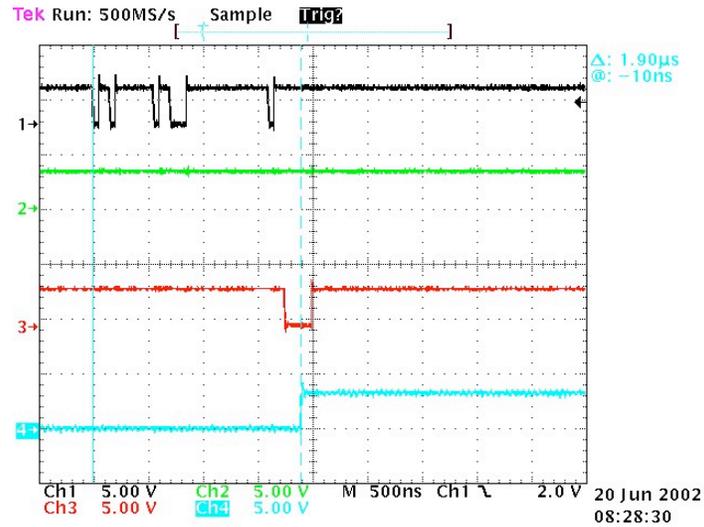
The maximum processing time for a trigger command (default settings) is shown below at approximately 27200 nsec.



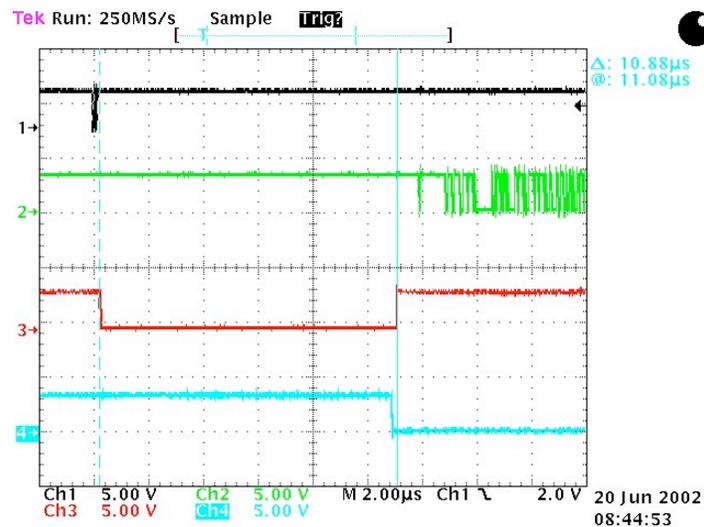
It is noted that delays which affect the HOLD or ADC readout time are reflected in the overall trigger processing time.

The GAFE calibration strobe for test charge injection is also controlled via the GARC command processor. In the following plots, channel 1 is the GARC command data, channel 2 is the GARC return data, channel 3 is the command processor Live time, and channel 4 is the GAFE STROBE signal.

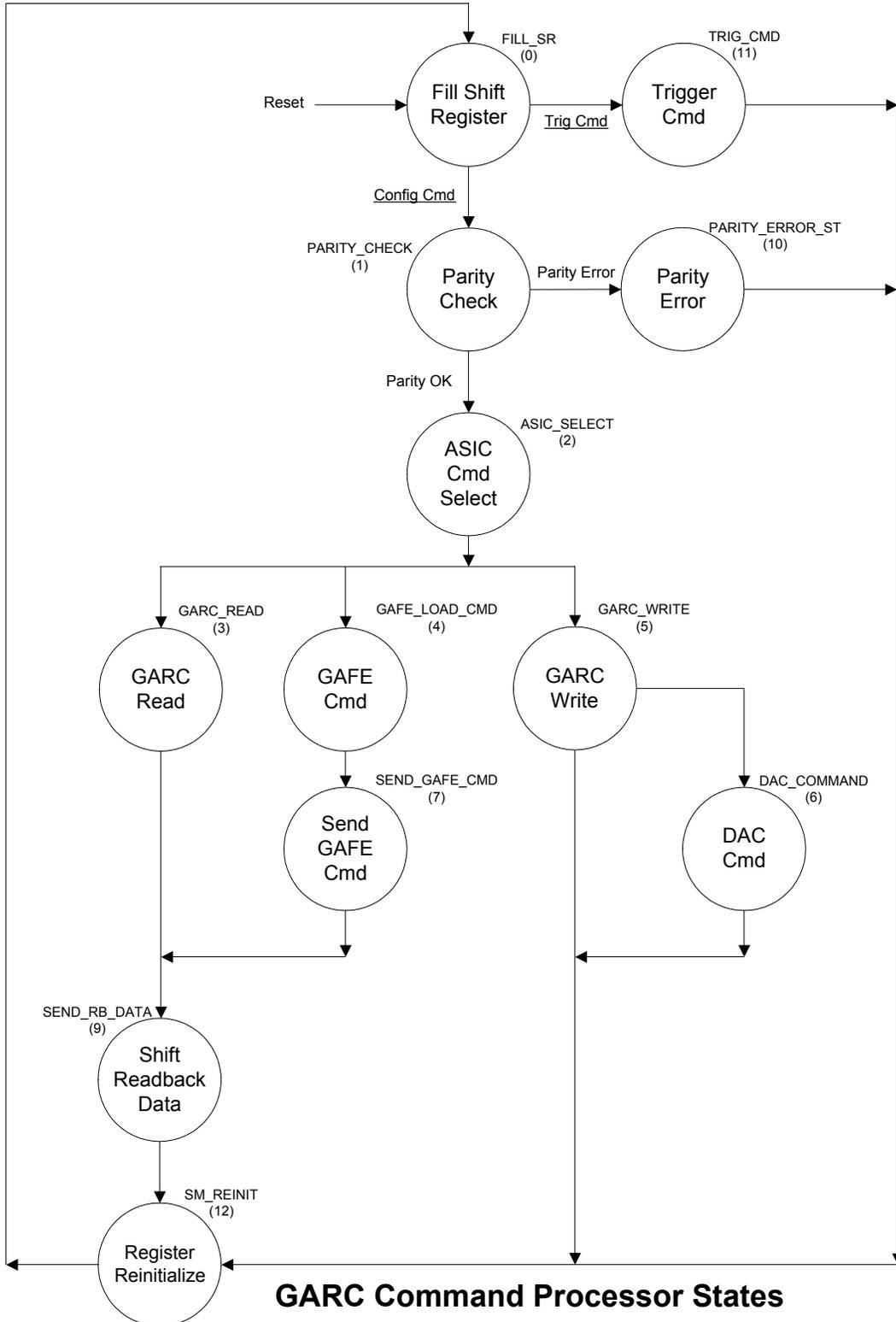
In the plot below, the GARC calibration command executes in 1750 ns from the leading edge of the first command bit. The Live signal is inactive for 250 ns. 150 ns after the deassertion of Live, the STROBE signal is activated.



This plot shows the execution of the calibration command and the STROBE (channel 4) signal transitioning active high. The STROBE signal stays active until a trigger is received and there is an ADC end of conversion. This is shown in the scope trace below.



A diagram of the command processor state machine is shown below.



Commands to the MAX5121 DAC are handled as a special case of the GARC write. The output level of this DAC is used to control the HVBS output. The MAX5121 DAC has the following 16 bit command format:

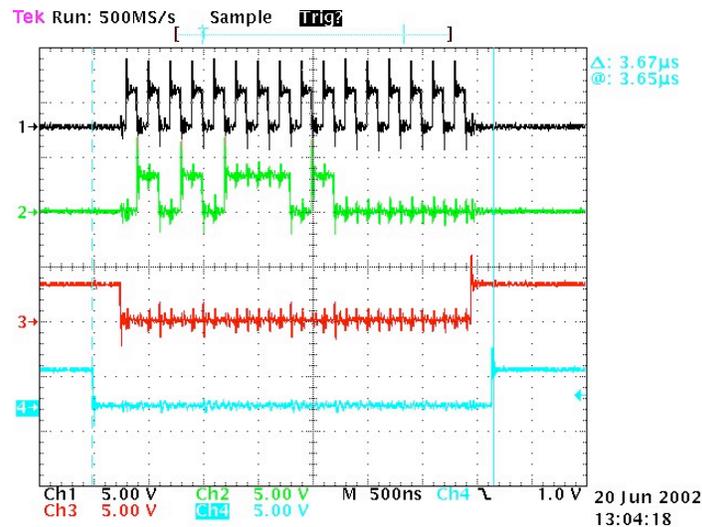
ccc	dddd	0
15:13	12:1	0
Configuration Control	DAC Data	

MAX5121 COMMAND FORMAT

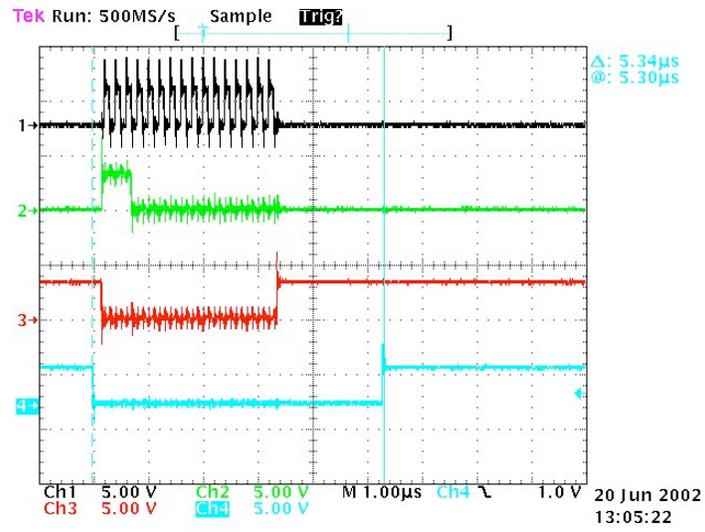
The configuration pattern ACD uses for a DAC write is 0-1-0. The DAC clock is sent at 5 MHz (derived from the 20 MHz ACD system clock). The command sequence is as follows:

- (1) Start with CS_N inactive hi, SCK low
- (2) CS_N goes active low
- (3) Send 16 SCKs to the DAC.
Data format is C2-C1-C0-D11-D10-D9-D8-D7-D6-D5-D4-D3-D2-D1-D0-S0
(where C2-C1-C0 == 0-1-0 and the sub-bit S0 == 0)
- (4) When SCK is lo, raise CS_N inactive hi

The DAC write command is shown in the plot below. Channel 1 is the DAC clock, channel 2 is the DAC data in, and channel 3 is the DAC chip select. Channel 4 is the GARC Live signal showing a dead time of approximately 3650 ns.



A DAC readback command is accomplished by sending a fixed pattern, 16'hE000, to the DAC and capturing the shift register output from the DAC. Specific details on the control options of this part are available from the manufacturer. The DAC readback cycle is shown below. The GARC command processor indicates a dead time of approximately 5300 ns for this command.



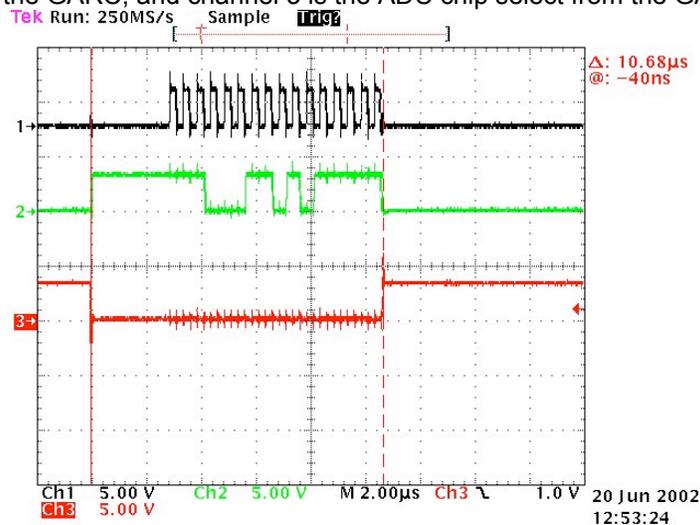
5.2.2.1.14 ADC and Zero-Suppression Logic

The PHA logic modules (garc_pha_logic.v) provides the control and data capture for the 18 MAX145 analog-to-digital converters (ADC) on the FREE circuit card. The Zero-Suppression (ZS) function is also performed in this module.

At the initiation of a trigger, a delay counter is started. At the finish of the delay counter the HOLD signal is transmitted from GARC to the GAFEs to transition the shaping amplifier track and hold circuit to the hold mode. The command processor then initiates an analog-to-digital conversion by activating the internal GARC signal “start_pha”.

Upon receipt of the “start_pha” signal, the PHA logic module activates the chip select on the ADCs. The GARC then waits the mandatory 2.5 usec required by the MAX145. Then, 16 cycles of ADC clock are provided at 2 MHz to the MAX145s, which is run in the external clock mode. All ADCs are run in parallel for every trigger. During the clocking of the ADCs, the GARC is shifting the returned 12 bits of PHA into registers. The GARC also latches the state of the channel id bit, CHID, of each GAFE into the MSB of each PHA register. At the end of conversion, the ADC chip select is returned to inactive high. The 18 registers of PHA, each 13 bits wide, is made available to the event data module via a multiplexer controlled by event_data.

The ADC readout cycle is shown on the oscilloscope plot below. Channel 1 is the ADC clock, channel 2 is the ADC data out to the GARC, and channel 3 is the ADC chip select from the GARC.



The PHA logic module also performs the ZS function combinatorially. Each captured PHA value is compared with a commandable preset register, PHA Threshold, and the result is available for transmission by the event data module. Each ADC channel has individually presettable threshold levels. A “1” indicates that the PHA value from the ADC is greater than the preset threshold.

The GARC also contains a register with 18 bits of PHA enable to allow the LAT to selectively enable or disable PHA readout of individual channels. This is intended to be used to turn off noisy channels in the nominal zero-suppressed mode. Another way to do this would be to raise the PHA threshold above the noise level. Note that if the CHID (i.e., analog range) bit is set to “high” the PHA value is automatically above threshold and will not be zero-suppressed.

5.2.2.1.15 Event Data State Machine

The event data state machine multiplexes and telemeters data to the AEM in response to an event trigger. The following data are sent in the event data word:

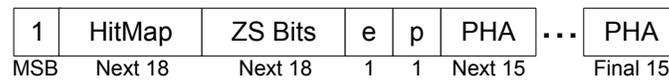
The 18 bit HitMap

The 18 bit Zero-Suppression (ZS) Map

PHA words, each 15 bits (0 to 18 PHA words may be sent)

For every trigger, the HitMap and ZS Map are sent. If the trigger type is non-ZS, then all 18 PHA values up to the value of MAX_PHA are transmitted. If the trigger type is ZS, then all PHA with an active bit (up to the number MAX_PHA) are transmitted. In the PHA readout, the lower number GAFE channels (e.g., 0) precede the higher numbered channels.

The event data format is as follows:



Start Bit = 1

Next 18 Bits = HitMap

Next 18 Bits = ZS Map

Next Bit = Cmd/Data Error Bit

Next Bit - Header Parity, odd over previous 37 bits

Next (15 bits * n) - PHA words

EVENT DATA FORMAT

The 15 bits PHA format is constructed by the event data processor as follows:

- Bit 14: 1 if more PHA to follow, 0 if this is the last one
- Bit 13: 1 if this is an HLD PHA, 0 if this is a low range PHA
- Bits 12-1: PHA data value, 0 to 4095
- Bit 0: Odd parity over previous 14 bits

5.2.2.1.16 GARC to GAFE Interface

Each GAFE interfaces to the GARC with the following signals

GAFE Signal	GARC Signal	Function	Notes
HOLD (+/-)	GAFE_HOLD (+/-)	Track-and-Hold control signal	One GARC signal to 18 GAFEs
STROBE (+/-)	GAFE_STROBE (+/-)	Calibration strobe	One GARC signal to 18 GAFEs
CMDD (+/-)	GAFE_CMDD (+/-)	GAFE Command Data	One GARC signal to 18 GAFEs
CMDCK (+/-)	GAFE_CK (+/-)	GAFE Command Clock	One GARC signal to 18 GAFEs
CHID	CHID_00 through CHID_17	GAFE Range ID bit	One signal from each GAFE ASIC
VETO	VETO_00 through VETO_17	VETO discriminators	One discriminator from each GAFE ASIC
IRTN	IRTN_00 through IRTN_17	Pseudo-LVDS interface current return	One return to each GAFE
HLD1, HLD2	HLD_OR, HLD_IRTN	High Level Discriminator	18 GAFE signals are OR'd to 1 GARC signal

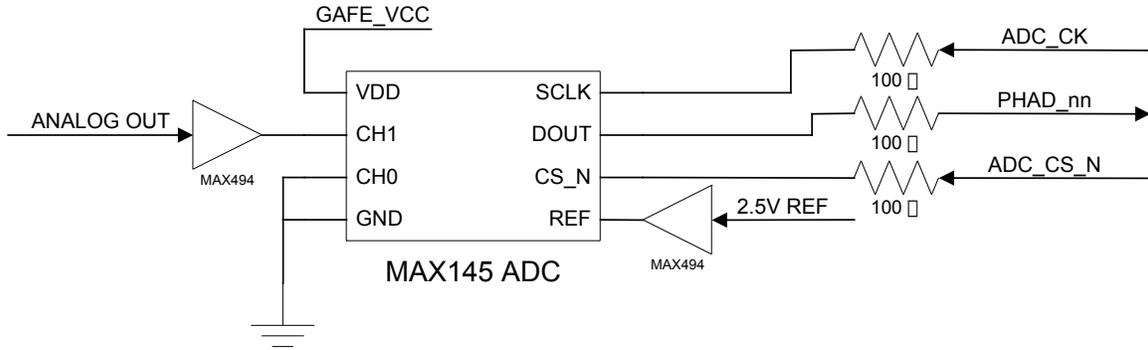
The four differential signals (HOLD, STROBE, CMDD, CMDCK) are common to all 18 GAFE ASICs. There is a single termination on the FREE board to generate the differential voltage required by the individual GAFE receivers.

Each GAFE sends a CHID and a VETO signal to the GARC on a pseudo-LVDS low current interface. The IRTN signal provides the current return for these signals. The current in the drivers is nominally 200 μ A.

Each GAFE has a high-level discriminator output. On the FREE circuit card, these signals are all bussed together to construct a wired-OR configuration. A single wired-OR HLD signal is received by the GARC. This is used by the GARC to generate a single board-level CNO signal.

5.2.2.1.17 GARC to ADC Interface

Each MAX145 receives identical control signals from the GARC. The ADC clock (ADC_CK) and the ADC chip select (ADC_CS_N) are common to all 18 GAFE from one GARC pin. Tanner PadOut cells drive these nodes. The clock operates at a nominal 2 MHz. The data out of each ADC drives an individual GARC pin with a Tanner PadInC cell as the receiver. All ADC conversions and data capture proceed in parallel. Each of the ADC-to-GARC signals is isolated via a 100-ohm series resistor. A simplified schematic of this interface is shown below.



GARC Digital Interface to the ADCs (1 of 18)

5.2.2.1.18 GARC to DAC Interface

The GARC interfaces to one MAX5121 DAC. There are a total of 4 inputs (DAC_CS_N, DAC_CLR_N, DAC_DIN, DAC_SCK) and 1 output (DAC_DOUT). The inputs to the DAC are driven from the GARC with a PadOut cell and isolated with a 100-ohm resistor as shown in the ADC interface above. The DAC_DOUT is received with a Tanner PadInC cell after a 100-ohm resistor. The DAC is clocked at a nominal 5 MHz.

5.2.2.1.19 Operation of the HVBS

The GARC command processor controls the operation of the HVBS. The GARC command processor controls the operation of the digital HV_ENABLE levels and the loading of the MAX5121 DAC which supplies the analog control voltage.

There are two HVBS, designated as HVBS 1 and HVBS 2, that the GARC controls. Writing to the GARC_Mode register controls these bits. The HVBS Enable bits are considered to be critical functions and are therefore implemented with a passive Triple-Modular-Redundancy (TMR) architecture (e.g., 2 or more wins).

- To enable HVBS #1, bits [3:1] of the GARC_Mode register are written as 3'b111.
- To disable HVBS #1, bits [3:1] of the GARC_Mode register are written as 3'b000.
- To enable HVBS #2, bits [6:4] of the GARC_Mode register are written as 3'b111.
- To disable HVBS #2, bits [6:4] of the GARC_Mode register are written as 3'b000.

The control of each bias supply is independent of the status of the other. The default state at reset for each of the six control bits is disabled. The design of the HVBS is such that the HV output is held near ground whenever the control bit is in the disabled state.

The output of the DAC value is used to control the output voltage of the HVBS when the supply is enabled. A DAC output for a register value of 0 corresponds to 0V on the HV output while a register value of 12'hFFF corresponds to the maximum HV output. Note that the register which controls the actual HV output voltage is contained in the MAX5121 DAC and not the GARC. Both HVBS receive the same analog voltage level.

There are two places where the values to be transmitted to the DAC register are stored in the GARC. One is the "HVBS Level" register and the other is the "SAA Level" register. These are two separate DAC settings, one for nominal operations and one for reduced-voltage operations whenever the ACD is transitioning through the South Atlantic Anomaly. GARC commands to these registers do not change the

value of the DAC but instead change the values to be used during these two instrument operational modes.

There are two commands that load the DAC register, "Use HV Normal" and "Use HV SAA". When these commands are sent, the DAC register is loaded with the respective register value. During flight, the DAC register will nominally be loaded twice per orbit (i.e., once entering SAA and once leaving SAA). This will provide a form of memory scrubbing for the MAX5121 part to mitigate SEU probabilities.

The GARC registers "HVBS Level" and "SAA Level" may be read back from the GARC and checked for accuracy prior to sending one of the "Use HV" commands.

When a GARC read command is sent to one of the "Use HV" addresses, the contents of the shift register in the MAX5121 is read back into the GARC and transmitted as configuration readback data. The MAX5121 provides only a "correct" readback the first time after the DAC is written. A complete understanding of the way the MAX5121 reads its data back is available in the Maxim datasheet.

5.2.2.1.20 Operation of the GAFE Calibration Strobe

The operation of the calibration strobe command, CALIB, is controlled by the GARC command processor. The CALIB strobe goes active 1750 ns after the leading edge of the first command bit of this command. The CALIB strobe will stay active until a trigger is received, processed, and an ADC end-of-conversion occurs. The command processor will be ready to receive another command 250 ns after CALIB goes active.

The intent of this command is to send a CALIB command (which initiates a GAFE test charge injection) and then follow this closely with a TRIGGER command to capture and hold the charge present in the analog system.

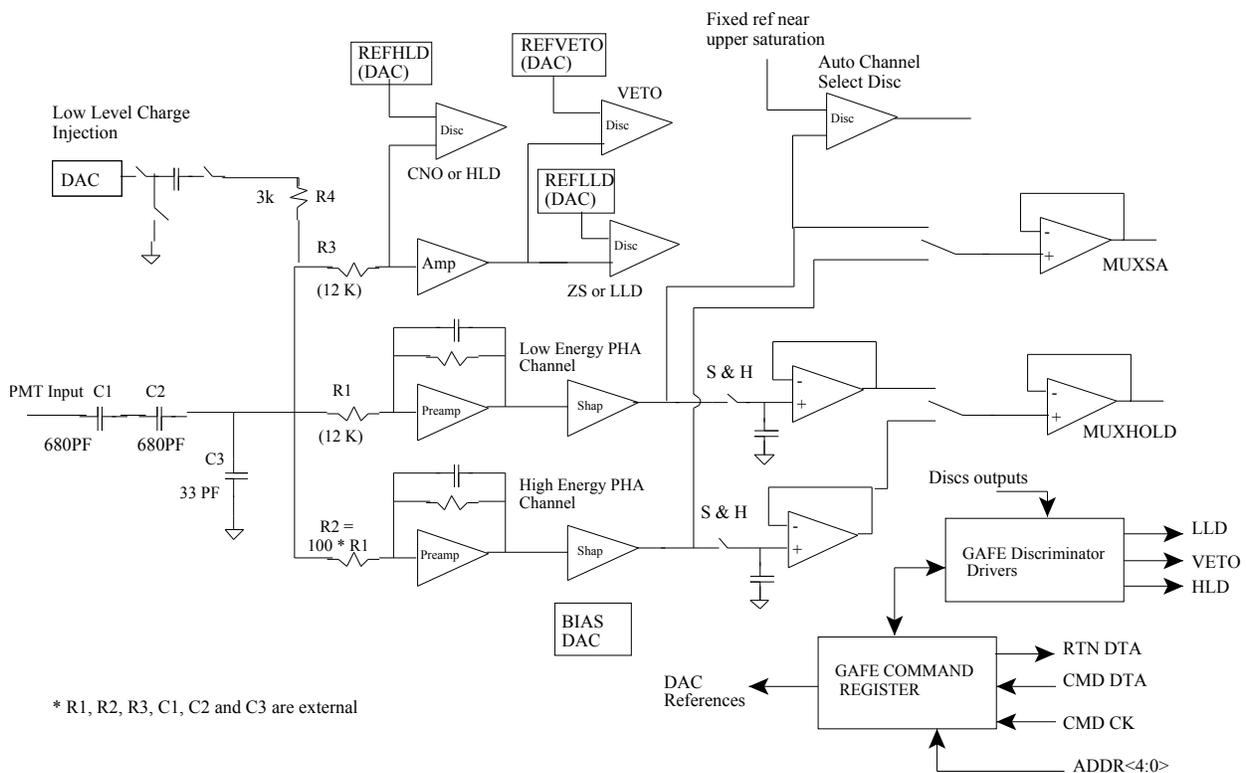
5.2.2.2 Analog ASIC (GAFE)

The primary purpose of the ACD Front End Electronics ASIC is to receive the PMT signal, and process it after suitable amplification to generate fast triggers or discriminator outputs, and shape and hold the signal for Pulse Height Analysis (PHA). The triggers that need to be generated are the VETO, the LLD or ZS, and the HLD or the CNO triggers.

In addition to the above analog circuits, this ASIC also contains the DACs to generate the various thresholds and biases, and also the digital modules which control the mode of operation of the chip and allow it to be interfaced to the outside electronics. The analog and digital subcircuits are described next. A simplified block schematic of the ASIC is given in the figure below.

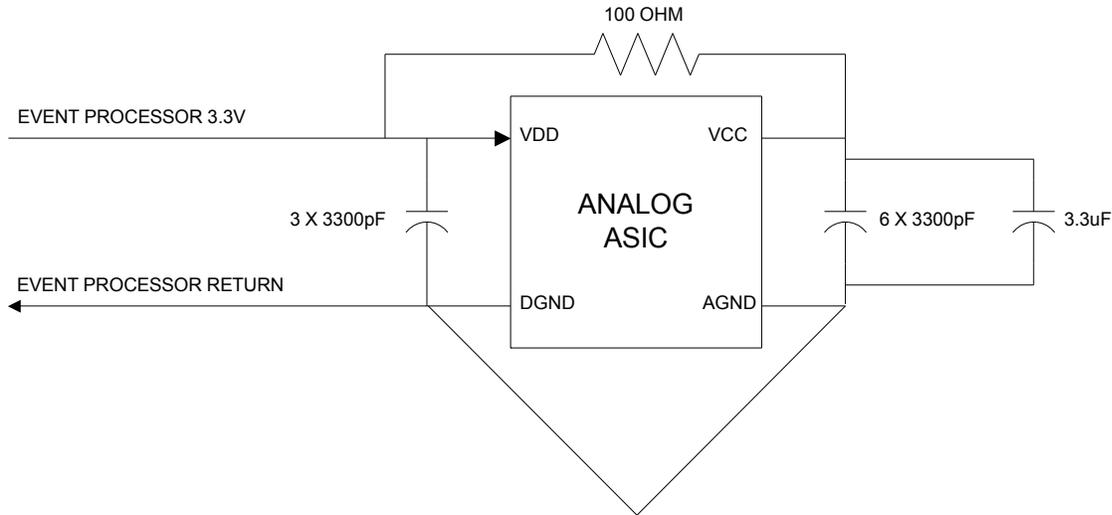
The analog front end comprises mostly of amplifiers and discriminators along with multiplexers, buffers and some other circuit modules. The main requirements that govern the front end electronics design are:

- The dynamic range of 0.1 to 1000 MIP, which for a PMT gain of 400,000, translates to 0.064 PC to 640 PC. The is a dynamic range of 1:10,000.
- Generation of a fast VETO trigger, preferably within 200ns for a 1 MIP signal
- The desired peaking time for the PHA signal is 3us, a shorter time is not desirable as it will lead to greater errors due to timing jitter of the Sample Hold signal.



GLAST ACD Front End (GAFE) Analog ASIC : Conceptual Diagram

The power supplied to the GAFE is as follows:



The +3.3V power from the AEM comes to the FREE circuit card. After local passive filtering on the FREE circuit card, this 3.3V is VDD, the digital power rail. This is locally bypassed with several ceramic capacitors (check with Dave about the values and suitability of 3300 pf caps). The ASICs analog power, VCC, is isolated by a 100-ohm resistor, and locally bypassed by ceramic capacitors and one tantalum capacitor.

5.2.2.2.1 GAFE Level IV Requirements

Detector: PMT, gain = 400,000 The GAFEs anode_output (negative charge) must process signals in the range 0.1 MIP to 1000 MIPS

Charge Range: 0.1 MIP to 1000 MIPS
 instrument dynamic range = 1 : 10,000
 MIP \Leftrightarrow 1 Photo electron (pe) \Leftrightarrow 1.6 E-19 Coulombs
 dynamic range = 1.6E-19 C to 1.6E-15 C

Detection of Charged Particles (L3 – 5.2): Generate a trigger output for signals above a nominal threshold of 0.3 MIPS

VETO Threshold (L4 – 5.3): Adjustable from 0.1 MIP to 2.0 MIP with a step size of 0.05 MIP or a charge range of 0.064pc to 1.28pc with a step size of 0.032PC

Veto Trigger Latency: latency for the entire ACD electronics chain shall be greater than 100 ns and less than 600ns from the time of particle passage., The minimum latency expected is 150ns and is not likely to be less than 50ns. The jitter on the Veto trigger shall be less than or equal to 200 ns.

VETO Duration: longer than the time for baseline recovery to 0.05 MIP (for a 2.0 volt signal amplitude that is generated from a 10 MIP signal.)

Recovery to 1 MIP: For 1 MIP signal, VETO should be no longer than 1.2us

Recovery to Large Signals (1000 MIPS): VETO should be no longer than 10 us

VETO Signal Retrigger (Pulse Pile Up !) : To be retriggerable within 50ns of the trailing edge.
(This should be handled by a VETO stretching Logic as described in the following text, this logic will be outside the ASIC)

CNO or HLD or High Level Threshold Detection: nominal threshold of 25 MIPS

CNO or HLD Threshold: Adjustable from 20 to 64 MIPs in steps of less than or equal to 1MIP

CNO or HLD Latency: latency no more than that of VETO signal.

LLD or ZS (Low Level Threshold or Zero Suppress) Signal: nominal threshold of 0.1 MIP

LLD or ZS Threshold: Adjustable from 0.05 MIP to 1 MIP in steps of 0.05 MIP

PHA (Pulse Height Analysis) output:

Low Energy / High Gain Channel:

Range: 0 to 10 MIPs

Resolution: 0.1 MIP to 10 MIPs with a precision of 0.02 MIP or 5% which ever is larger

High Energy / Low Gain Channel:

Range: 0 to 1000 MIPs

Resolution: for pulses above 20 MIPs and up to 1000 MIPs, a precision of 1 MIP or 2% which ever is larger

Test Charge Injection: ASIC to have mechanism for injecting test charge at the front end of electronics chain, the maximum injected charge will be 40pc (16pf * 2.5v), which corresponds to 62.5 MIPs.

Digitization: 10 or 12 bit ADC outside ASIC

5% Integral Non Linearity acceptable

PMT Rise Time: for signal out of PMT : 3-5ns, 1ns for faster tubes

Event Rate: < 3 KHz per PMT

<= 5% of PMTs are expected to be digitized on an average

The various blocks of the analog circuit which are shown in Fig. ??? are discussed next

5.2.2.2 Amplifier with Charge Splitting

The ACD requirements of 0.1MIP to 1000 MIPs dynamic range is too large to be handled by one channel of electronics with a fixed gain. To ease this requirement on electronics, the electronics are split into two channels, a high gain channel that can measure up to 10 MIPs, and a low gain channel that can measure up to 1000 MIPs. In this approach two preamplifiers are used and each has a series resistance at the input to the PMT. The charge that goes into each of the preamplifiers is inversely proportional to the resistance. This technique is used to handle a wide dynamic range such as required here.

In addition to the charge splitting resistances, an external cap of 33 pF is used. The two charge splitting resistances bleed the capacitor's charge. The resistors are in series with two amplifiers. The amplifiers are part of a slow shaping circuit that is required for PHA. The voltage signal developed across the capacitor is fed to the input of the discriminator through a series resistance. For this approach, the charge splitting resistors and capacitors are external to the GAFE.

5.2.2.3 Input Charge

The design requirement calls for handling a signal range from 0.1 MIP to 1000 MIPs. A signal of 0.1 MIP generates 1 photoelectron (pe), which has a charge of 1.6E-19 Coulombs (C). Therefore, for a full scale input of 1000 MIPs, the charge generated is 1.6E-15 C. Since the gain of the PMT is 400,000, the charge input to the ASIC is, 0.064PC for 0.1 MIP, and 640 PC for 1000 MIPs. For a charge collection capacitor of 33 pF, the signal developed across it as required by the various discriminators is as follows:

0.1 MIP <=> 0.064 PC <=> 1.94 mV
1 MIP <=> 0.64 PC <=> 19.4 mV
10 MIPs <=> 6.4 PC <=> 194 mV

30 MIPs \Leftrightarrow 19.2 PC \Leftrightarrow 582 mV
50 MIPs \Leftrightarrow 32 PC \Leftrightarrow 970 mV

The choice of 33 pF for the external charge collection capacitor therefore seems to be adequate as the voltage generated across it is within the input range of all the discriminators.

5.2.2.2.4 High Voltage Coupling Capacitors

Since the charge is collected across a capacitor of 33 pF, the high voltage capacitors should be much larger than 33 pF. Using two 680 pF capacitors in series for high voltage decoupling is adequate.

5.2.2.2.5 Input Time Constant and Discriminator Output Duration

The design requirement for the fast VETO signal is 1.2 μ s for a 1 MIP signal. Therefore, the longest VETO duration obtained for the minimum threshold of 0.1 MIP is given by the equation,

$$0.1 \text{ MIP} = 1 \text{ MIP} * \exp^{-1.2[\mu\text{s}/\tau]} \Rightarrow \tau = 0.43 \mu\text{s}$$

Therefore, the time constant chosen for a signal going into the discriminators is 400 ns. This implies that the series resistance to the input of the low energy Shaping amp is given by,

$$r1 = 400 \text{ ns} / 33 \text{ pF} = 12 \text{ k}\Omega$$

5.2.2.2.6 Charge Splitting Resistors

As discussed above, the input resistor to the High gain or the Low Energy channel is 12 k Ω . The High Energy channel has the full scale of 1000 MIPs, which is 100 times the full scale of Low energy channel. The series resistance to the High energy channel's input is chosen as 100 times that of the resistance in the Low energy channel and is 1.2 M Ω .

5.2.2.2.7 Shaping Time for Pulse Height Amplifiers

The latency of the sample and hold from the LAT is 2 μ s. Therefore, the minimum peaking time of the shaped pulse is 2 μ s. However, the resistor and capacitors that are fabricated in silicon can vary by 20% from one run to another and in the x and y direction. As a result, the peaking time has been increased by $2 \mu\text{s}/0.8/0.8 = 3.125 \mu\text{s}$.

5.2.2.2.8 Fast Channel Amplification

Where the VETO and Low Level (LLD) discriminators trigger, the signal range is small. The signal across the input capacitor is first amplified by a gain of 20 before being input to the VETO and LLD comparator circuits. With reference to 3.3 volts, a 0.1 MIP signal after amplification of 20 would now correspond to approximately 40 mV. That is large enough to trigger the comparator.

The input to the High Level (HLD) or CNO discriminator is not amplified, as the signal is already large enough.

5.2.2.2.9 Low Level Test Charge Injection

An on chip capacitor of approximately 16 pF has been fabricated. For a 2.5 v input, this would allow charge injection of 40 PC or 62.5MIPs. When not in use, the charge injection capacitor is disconnected by a switch that is activated by the Test Enable signal.

5.2.2.2.10 Zero Suppression and Low Level Discriminator

The threshold of this discriminator is set by a signal labeled, "REFLLD". Since the signal is negative going at the discriminator input and is at a base line of vdc1 (approx 1.5v), the reference is set to a level below

vdc1. Therefore for zero level threshold setting, the reference should be set to vdc1 and for increasing signals; it should be decreased towards zero volts. The threshold setting is done by on chip DAC.

5.2.2.2.11 VETO Discriminator

The threshold of this discriminator is set by signal labeled, “REFLLD”. Since the signal is negative going at the discriminator input and is at a base line of vdc1 (approx 1.5v), the reference is set to a level below vdc1. Therefore for zero level threshold setting, the reference should be set to vdc1 and for increasing signals; it should be decreased towards zero volts. The threshold setting is done by on chip DAC.

5.2.2.2.12 High Level Discriminator or CNO

The threshold of this discriminator is set by signal labeled, “REFHLD”. Since the signal at the discriminator input is at a base line of vdc1 (approx 1.5v), the reference is set to a level below vdc1. Therefore for zero level threshold setting, the reference should be set to vdc1 and for increasing signals, it should be decreased towards zero volts. The threshold setting is done by on chip DAC.

5.2.2.2.13 PMT Gain Drift

There is no gain adjustment on the ASIC. However, the gain of a group of PMTs is increased by increasing the high voltage so that the gain of the weakest PMT in that group is brought back up to the nominal level. To take care of the PMT gain variation from channel to channel, the threshold of the various discriminators for each channel or PMT are individually set by the on chip DACs.

A one time gain adjustment of the electronics chain is also possible by suitably selecting the external charge collection capacitor which is to be implemented on the board as a parallel combination of two capacitors.

5.2.2.2.14 Low Energy Pulse Height Analysis Channel

The low energy signal is amplified, shaped to peak at 3 μ s and feeds a sample hold circuit which is operated when a Hold signal is delivered from external to the chip.

5.2.2.2.15 High Energy Pulse Height Analysis Channel

The high-energy channel is similar to the low energy channel. The signal is amplified, shaped to peak at 3 μ s and feeds a sample hold circuit which is operated when a Hold signal is delivered from external to the chip.

5.2.2.2.16 Sample and Hold

The sample and hold comprises of a simple switch in series with the output of the final stage of shaping amplifier and a hold capacitor as shown in fig. 1. During normal operation, the switch is kept closed and the voltage across the hold capacitor tracks the output of the shaping amplifier, and when the hold signal is applied the signal across the capacitor is held.

5.2.2.2.17 Shaping Multiplexer

There is an on chip analog multiplexer that selects the output of either the LE or HE shaping amp outputs. This multiplexer is provided for testing of the circuits and is not required during flight.

5.2.2.2.18 Hold Multiplexer

There is an on chip analog multiplexer which selects the output of either the LE or HE Sample and Hold outputs, the output of this multiplexer is passed to the external ADC for digitization. The selection of the low or high-energy channel can be performed in the Auto mode or the manual mode. In the auto mode, an on chip discriminator on the output of LE shaping amp senses if the signal is near the saturation and switches the multiplexer to HE channel. In manual mode, the channel selection is under external control.

5.2.2.2.19 Auto Mode Channel Selection Comparator

A discriminator is provided at the output of low energy shaping amp and is set slightly below the upper saturation of the signal. When this discriminator fires, signaling a large signal, the Hold multiplexer automatically switches to the high energy channel when the ASIC is set to Auto mode.

5.2.2.2.20 Threshold Settings

On-chip DACs are provided to set the various baselines and thresholds as needed by various sub circuits and discriminators. The DACs are described in the next section.

5.2.2.2.21 Digital-to-Analog Converters (DACs)

5.2.2.2.21.1 Overview:

The DACs are used to set the discriminator threshold as follows:

Signal	Min Setting	Max Setting	Step Size	No. of Bits
Veto	0 MIP	3.2 MIPs	0.05 MIP	6 bits
LLD	0 MIP	3.2 MIP	0.05 MIP	6 bits
HLD	0 MIP	64 MIPs	1 MIP	6 bits

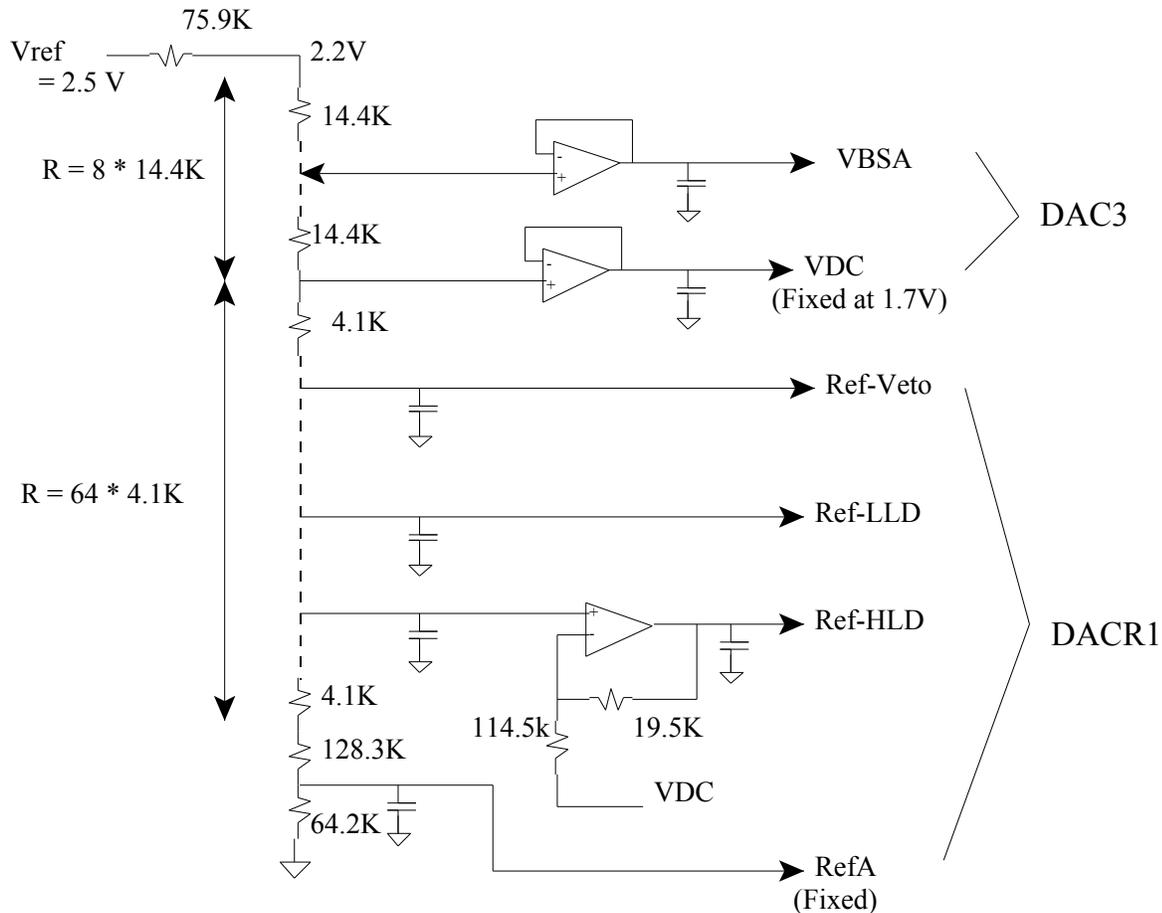
The Test Charge injection DAC is also a 6-bit DAC that sets the voltage level to the test charge injection between 0 and 2.5 Volt. The Base Line DAC is a 3-bit DAC that sets the baseline at the output of the Shaping Amps between 2.2 V and 1.75 V, the nominal setting is 2 V.

The DAC block also generates fixed voltages for the following:

- Disc Base Line level: This is set to 1.75 V, the signal going into all the discriminators have a dc offset of this value of 1.75 V. The signal going into the discriminators is an inverted exponential in shape, and therefore the various thresholds are set below this baseline.
- Auto Channel Select Discriminator Level: This is set to 0.8 V. When the signal in the low energy channel has exceeded the difference between this voltage and the DC base line at the shaping amp out, then the auto channel discriminator fires and this is used to switch the PHA to the high-energy channel.

5.2.2.2.21.2 The DAC architecture:

The DACs are implemented using a resistive divider chain as shown in the figure below. There are three DAC modules on the ASIC, DAC3 provides the level for the baseline at the output of the



An Overview of the DAC architecture in GAFE ASIC

Shaping amps and that at the input to the discriminators. DACR1 provides the threshold references for the discriminators. DACT provides the reference level for the on chip Test Charge injection circuit. As shown in figure ???, the DACs are formed using a resistive chain. DAC3 and DACR1 are in series with voltage reference which is set at 2.5 V. DACT is a separate chain of 64 resistors across Vref and ground, the output of this DAC determines the level of on chip Test charge injection. The structure and functioning of the various DACs is described next.

5.2.2.2.21.3 DAC3: VBSA and VDC generation

The DAC3 is a 3-bit DAC that is formed by a series of 8 resistances each of 14.4K. This DAC is in series with a 75.9K resistor connected to the Vref, which is set at 2.5V. The bottom end of the resistive chain is connected to the resistive chain for the 8-bit DACR1.

VBSA: The 3-bit DAC input is applied to a 3-bit to 8 line decoder module that selects one of the 8 nodes in the resistive chain. The output of this resistive chain is buffered and made available as VBSA, which is used to set the baseline at the output of shaping amps used for PHA. The nominal value of VBSA is 2 V. This level can be set between 1.7 V and 2.2 V using the 3-bit DAC.

VDC: This voltage is fixed to 1.7 V approximately and is made available from the bottom of the resistive chain comprising DAC3. This level determines the baseline at the input to the discriminators used to generate the various triggers.

5.2.2.2.21.4 DACR1: Threshold settings for Veto, LLD, HLD and PHA range select

This DAC comprises of 64 resistors in series. There are three 6-bit-to-64-line decoders to independently select the threshold for each of the Veto, LLD and HLD. The level for PHA range select is fixed. Since this DAC is in series with DAC3 or the bottom node of DAC3, which determines the VDC level, the threshold settings are always guaranteed to be relative to the baseline (VDC) and therefore any drift in the baseline is not going to affect the performance of the discriminators.

Veto & LLD: Veto and LLD thresholds are set able in 64 steps with 6-bit DACs. Since these thresholds are set to real low levels of the incoming signal, the signal from the PMT is first amplified by 20 before being fed to the Veto and LLD discriminators.

HLD: This sets the high-level discriminator threshold. This is a 6-bit DAC, which allows for 64 steps of settings.

Since the pulses are inverted, a signal of greater amplitude means setting the threshold farther below the baseline of VDC. The DAC setting of x3f or all "1"s, will set the threshold at the top or at VDC, which would actually mean a signal amplitude of zero. Conversely, a DAC setting of all "0"s would set the threshold at the bottom of the DAC which would correspond to full scale signal. Therefore the DAC bits should be set to x3f less the desired signal amplitude setting.

RefA: PHA range select threshold: This is a fixed voltage set near the full scale of the PHA. When the signal in the low energy channel PHA exceeds this threshold, the output of this discriminator is used to select the High energy channel for PHA. This level is presently set to 0.75 V.

5.2.2.2.21.5 DACT: Test Charge injection DAC

This DAC is also a 64 series resistor DAC strung across the Vref of 2.5 volts and ground. This 6-bit DAC determines the level of the test charge injection. An on chip capacitor of approximately 16 pF has been fabricated, for a 2.5 V input, this would allow charge injection of 40 pC or 62.5 MIPs.

5.2.2.2.22 GAFE Logic Module

The GAFE ASIC contains a digital module that controls the various functions of the ASIC. The digital interface is through a serial data bus, which comprises of a received data, return data and a clock. This serial link is implemented using low voltage differential signals; the chip is selected by an address ID for which there are 5 address pins available. The main function of the serial link is to program the various DACs, and set a few other parameters. The ASIC also outputs the various discriminator levels in a low voltage differential form, however to save on pins, the returns of some of the signals are tied together to form a common return. In addition, the digital module also selects the multiplexer channel to select either the high or low gain channel for PHA, controls the on chip test charge injection circuit, and operates the sample and hold.

5.2.2.2.22.1 Overview of the Logic Core

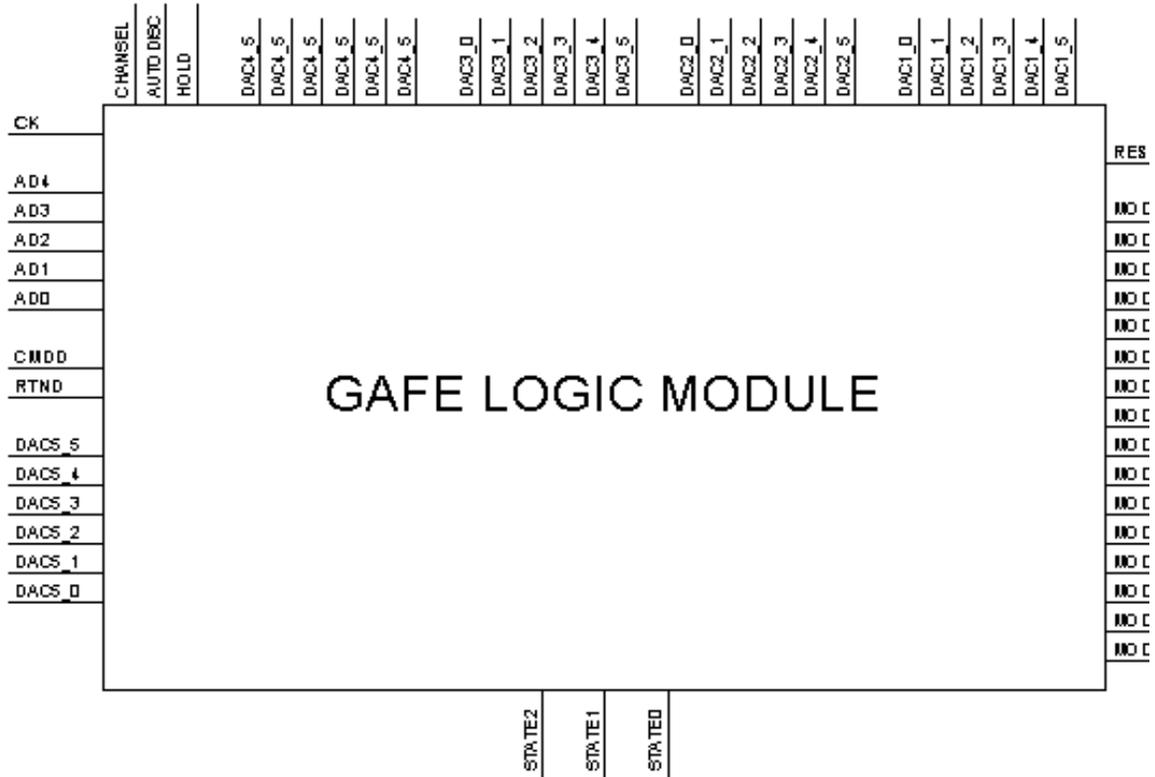
The design was done utilizing Verilog as the description language, Exemplar Leonardo Spectrum as the synthesis tool targeting the Tanner Agilent 0.5 μ m standard cell library, and Tanner L-Edit as the automated place and route layout tool. Core verification was performed via the Tanner LVS tool.

The GAFE logic has consists of a set of registers accessible via a command-response protocol. These registers may be written and read out by serial digital command. This serial data is GAFE_DAT and is clocked into the module on the positive going edge of GAFE_CLK.

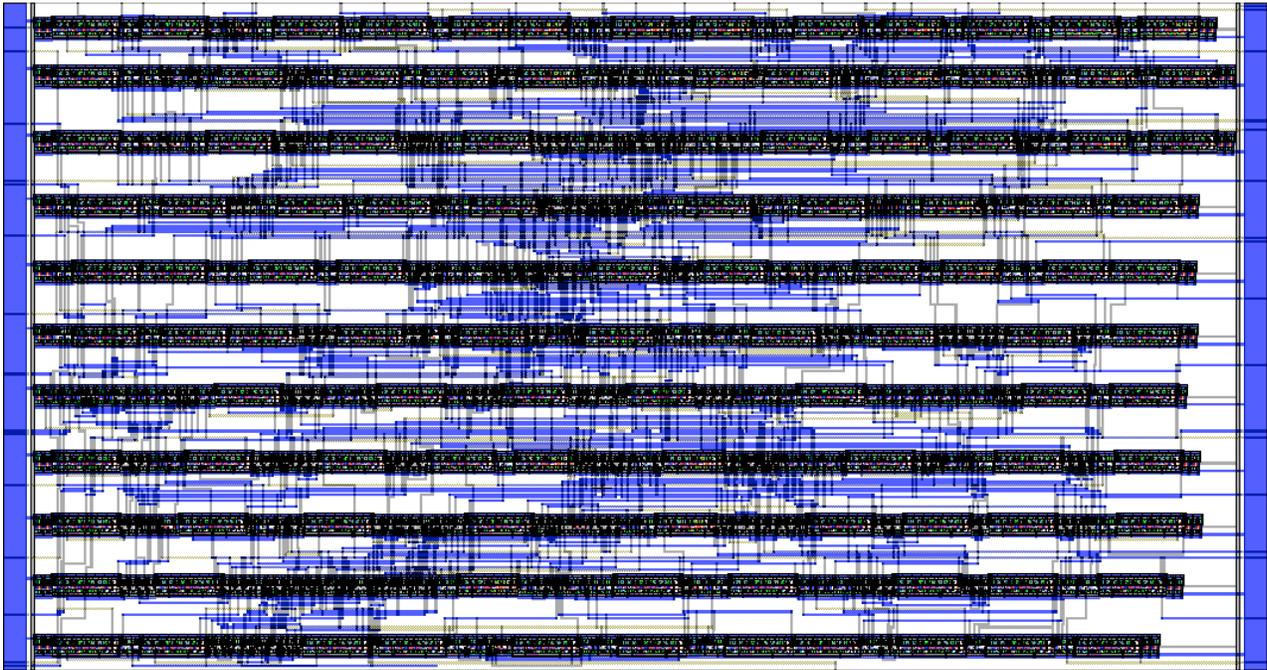
On a single FREE card, each GAFE has a unique address consisting of 5 voltage-level inputs, tied to either logic high or logic low through a series resistor. There is one 16-bit GAFE Mode register and five six bit DAC control registers (e.g., DAC1 – DAC5) available for configuration and are described below. There are five diagnostic commands available.

All GAFE commands originate in the LAT/AEM and pass through the GARC for formatting. Sufficient time is allowed by the GARC for one command to execute before the next GAFE command is sent. In the case of "Write" commands, this is at least 8 trailing zero bits. For "Read" commands, at least 28 trailing zero bits should be sent to allow for the full GAFE readback. This is controlled in the GARC by the garc_cmd_proc state machine.

A block diagram of the layout of the GAFE core logic module is shown below.



The physical layout of the GAFE logic core module is shown below.



5.2.2.22.2 GAFE Configuration Command Data Format:

The GAFE logic core responds only to properly structured commands. This format is detailed in the table below.

Bit(s)	Bit Description	Value
27	Start Bit	1
26	Read/Write Bit	0 = Write, 1 = Read
25:21	GAFE Chip Address	Hardwired inputs. Value 'h1F is reserved for broadcast write commands. Nominal values are 0 – 17 on FREE PCB.
20:17	GAFE Register Select	0: GAFE Mode Register[15:0] (read/write) 1: DAC_1 [5:0] (read/write) 2: DAC_2 [5:0] (read/write) 3: DAC_3 [5:0] (read/write) 4: DAC_4 [5:0] (read/write) 5: DAC_5 [5:0] (read/write) 6: Version (diagnostic: read-only) 7: Write Counter (diagnostic: read-only) 8: Reject Counter (diagnostic: read-only) 9: Loop Counter (diagnostic: read-only) 10: Chip Address (diagnostic: read-only)
16:1	GAFE Config Data	
0	Parity Bit	Odd parity over [26:1]

5.2.2.2.22.3 Contents of the GAFE Mode Register

The GAFE core contains one 16-bit register to be used for the static configuration of multiple modes. These bits are utilized in version 2 of the GAFE as detailed in the table below.

GAFE Mode Bit(s)	Description	"0" State	"1" State	Default
0	TCI Gain	Lo	Hi	0
1	TCI Pulse Enable	Disable	Enable	1
2	Autorange Select	Auto	Manual	0
3	Range Select	Lo	Hi	0
4	VETO Disc Enable	Disable	Enable	1
5	HLD Disc Enable	Disable	Enable	1
15:6	Spare Mode Bits	--	--	0

5.2.2.2.22.4 Description of the Diagnostic Readback Registers

Reading back register 6 provides the GAFE hardware version number in return data. For the May 2002 submission (GAFE_2), this number is 2. Reading back register 7 provides a count of the number of valid configuration commands written to the register. This is initially reset to 0 and rolls over at a count value of 63. Reading back register 8 provides a count of rejected commands since power up. This counter rolls over at 63. Reading back register number 9 provides a counter of the number of times the state machine loop has completed, also rolling over at 63. Register number 10 provides a readback of the hard-wired chip address.

5.2.2.2.22.5 GAFE Return Data Format:

The GAFE core returns configuration data when a valid readback command is received. The return data format is basic and listed in the table below.

Bit(s)	Bit Description	Value
16	Start Bit	1
15:0	GAFE Configuration Return Data	Mode register is 16 bits in length Other registers are padded with leading zeroes in the most significant bits.

5.2.2.2.22.6 GAFE Commands

The following table represents each of the available GAFE commands. In this table, **a** is the 5 bit hexadecimal chip address, **dddd** is the 16 bit hexadecimal data word, and **p** is the odd data parity. Note that a GAFE will process a write command either for the address hard-wired to the chip address pins or to an address of 'h1F'. A GAFE will process a read command only for an address identical to the hard-wired address. It is an operational constraint that, for any given ACD circuit board, each GAFE must have a unique address.

	GAFE Command Mnemonic	Command Pattern	Command Function
1	GAFE_Mode_Write	1 0 a 0000 dddd p	Write to the GAFE Mode Register
2	GAFE_DAC1_Write	1 0 a 0001 00dd p	Write to the GAFE DAC #1 Register
3	GAFE_DAC2_Write	1 0 a 0010 00dd p	Write to the GAFE DAC #2 Register
4	GAFE_DAC3_Write	1 0 a 0011 00dd p	Write to the GAFE DAC #3 Register
5	GAFE_DAC4_Write	1 0 a 0100 00dd p	Write to the GAFE DAC #4 Register
6	GAFE_DAC5_Write	1 0 a 0101 00dd p	Write to the GAFE DAC #5 Register

7	GAFE_Mode_Read	1 1 a 0000 0000 1	Read from the GAFE Mode Register
8	GAFE_DAC1_Read	1 1 a 0001 0000 1	Read from the GAFE DAC #1 Register
9	GAFE_DAC2_Read	1 1 a 0010 0000 1	Read from the GAFE DAC #2 Register
10	GAFE_DAC3_Read	1 1 a 0011 0000 1	Read from the GAFE DAC #3 Register
11	GAFE_DAC4_Read	1 1 a 0100 0000 1	Read from the GAFE DAC #4 Register
12	GAFE_DAC5_Read	1 1 a 0101 0000 1	Read from the GAFE DAC #5 Register
13	GAFE_Version	1 1 a 0110 0000 1	Read back the GAFE logic version
14	GAFE_Write_Ctr	1 1 a 0111 0000 1	Read back the GAFE Write Counter (diagnostic)
15	GAFE_Reject_Ctr	1 1 a 1000 0000 1	Read back the GAFE Cmd Rejects Counter (diagnostic)
16	GAFE_Cmd_Ctr	1 1 a 1001 0000 1	Read back the GAFE Total Commands Counter (diagnostic)
17	GAFE_Chip_Addr	1 1 a 1010 0000 1	Read back the GAFE Chip Address (diagnostic)

5.2.2.2.22.7 Auto-Discriminator Logic

An independent logic module is contained in the GAFE core. This is used to control the position of the shaping amplifier selection multiplexer. This logic is clocked by the positive edge of the HOLD signal. The values of the AUTODISC discriminator and GAFE Mode bits 2 and 3 are used to determine the control of the multiplexer to select either the low energy (LE) or the high energy (HE) channels. This flip-flop and control logic will be tested with the analog portion of the GAFE.

The channel selection indicator, the CHID pin, is not returned in the serial return data. Verification of this function will be performed with an oscilloscope in the analog verification procedure of the GAFE.

The logic for the multiplexer channel selection is as follows:

AUTODISC	Mode[2]	Mode[3]	Channel Select	Description
0	0	0	0	Auto, Lo
0	0	1	0	Auto, Hi
0	1	0	0	Manual, Lo
0	1	1	1	Manual, Hi
1	0	0	1	Auto, Lo
1	0	1	1	Auto, Hi
1	1	0	0	Manual, Lo
1	1	1	1	Manual, Hi

5.2.2.2.23 Pin Out

The various pins of the ASIC are described next. The ASIC has 48 bonding pads, the pin numbering starts from the top left and goes anticlockwise.

5.2.2.2.23.1 Supply Pins:

VCC: Pins: 1, 11: Analog Power, 3.3 V. These pins should have a 0.1 uf cap very close to the ASIC on the board the chip is mounted. If there is only enough space available for one 0.1 uf cap on the board, then it should be mounted close to pin 1.

Agnd: Pins: 2, 4, 6, 8, 12, 33, 35: Analog ground.

Vdd: Pins: 24, 38: Digital Power, 3.3V. These pins should have a 0.1 uf cap very close to the ASIC on the board the chip is mounted. If there is only enough space available for one 0.1 uf cap on the board, then it should be mounted close to pin 24

Dgnd: Pins: 13, 37,47. Digital ground.

5.2.2.2.23.2 Analog Pins:

salo: Pin 3: Slow Amp, Low Energy Input: This is the input for the low energy or high gain channel for the PHA. To this input, a 12K (R1) resistor is connected as shown in Fig.1. This resistor in conjunction with the R2 connected to sahi, splits the charge into two channels for PHA.

sahi: Pin 5: Slow Amp, High Energy Input: This is the input for the high energy or low gain channel for the PHA. To this input, a 1200K (R2) resistor is connected as shown in Fig.1. This resistor in conjunction with the R1 connected to salo, splits the charge into two channels for PHA.

discin: Pin 7: Input to the Fast channel for discriminators: To this a 12 K (R3) is connected as shown in Fig.1. This is a high impedance input to a fast shaping or large bandwidth amp. The output of this amp is to generate triggers for Veto and LLD.

Vref: Pin 9: 2.5 V Reference. This pin should be bypassed with a 0.1uf cap close to the ASIC. This is the reference input which is used by the DACs to generate the various discriminator thresholds and also is used to set the baseline for the shaping amps and of the signal that is input to the discriminators.

muxh: Pin 34: Multiplexer out for the Sampl and Hold outputs of the low and high energy PHA channels. This pin is connected to the ADC input.

muxsa: Pin 36: Multiplexer out for the shaping amp. This is the multiplexed shaping amp out for the low and high energy channels. This output is only meant for testing and diagnosis, it is not to be used on the final flight board.

tci: Pin 48: Test charge injection output. This is the charge injection output which is applied to the node where the two charge splitting resistances R1 and R2 meet, the connection to this node is via a 3k resistance is added as shown in Fig.1.

sparea: Pin 10: This is a spare pin associated with the analog modules.

5.2.2.2.23.3 The Digital Pins:

a0, a1, a2, a3, a4: Pns: 30, 31, 32, 44, 45 respectively: Address Pins: These pins are tied either to ground or to Vdd and determine the address or the ID of the ASIC.

LLD: Pin 29: This is the ZS or LLD out, this is a low voltage differential signal, but its return is in common with the Veto and Chnid. Having a common return, saves 2 pins per GAFE ASIC, and since there are 18 GAFE ASICs connected to one GARC ASIC, this results in a saving of 36 pins on the GARC.

VETO: Pin 28: This is the VETO out, this is a low voltage differential signal, but its return is in common with the LLD and Chnid. Having a common return, saves 2 pins per GAFE ASIC, and since there are 18 GAFE ASICs connected to one GARC ASIC, this results in a saving of 36 pins on the GARC.

chnid: Pin 27: A high indicates that high energy PHA channel has been selected for the multiplexed outputs. This is a low voltage differential signal, but its return is in common with the Veto and LLD. Having

a common return, saves 2 pins per GAFE ASIC, and since there are 18 GAFE ASICs connected to one GARC ASIC, this results in a saving of 36 pins on the GARC.

irtn: Pin 26: This is the common return pin for signals LLD, VETO and chnid.

HLD2 and HLD1: Pins 18 and 19 respectively. This is a pseudo-differential out of the High level discriminator. Across these two pins is switch, which is turned on when the discriminator is fired, otherwise it is off. The HLDs from all the GAFE ASICs are tied together to implement an “OR” gate. When the HLD on any one of the 18 GAFE ASICs fires, the impedance between the HLD2 and HLD1 is lowered, and this is sensed by the GARC chip.

reset: Pin 25: This is the reset pin for digital logic.

Hold+ and Hold- : Pins 23 and 22 respectively: These are the differential hold inputs which make the PHA sample and hold circuit to switch from tracking to Hold mode

Strob+ and Strob- : Pins 21 and 20 respectively: These are differential strobe inputs, the signal which cause the charge injection of the on chip test pulser.

cmdd+ and cmdd- : Pins 41 and 42 respectively: These are low voltage differential inputs for the command data to the digital control module on the ASIC.

cmdck+ and cmdck- : Pins 39 and 40 respectively. These are low voltage differential inputs for the command clock to the digital control module on the ASIC.

rtnd: Pin 14: This is the return data from the digital block of GAFE ASIC.

state0, state1, state2: Pins 17, 16 and 15 respectively: These are the test outputs from the digital section of the GAFE ASIC and are meant for diagnosis only.

spared0 and spared1: Pins 43 and 46 respectively: These are spare pins associated with the digital modules of the GAFE ASIC.

5.2.2.2.24 Interfacing Issues:

5.2.2.2.24.1 Veto stretching:

The veto coming out of the ASIC should be stretched by 0.2 μ s before it is passed on to the LAT, this allows 0.2 μ s for the comparator to recover and be in a ready state to fire again if another signal arrived on the trailing edge of the stretched veto pulse. Assuming that the FPGA or the digital logic outside the ASIC can retrigger instantly after the trailing edge, the dead time of the ACD electronics is now effectively zero seconds. However, since the electronics has finite rise, fall and delay times, there will be some finite time of dead time which will be unavoidable.

5.2.2.2.24.2 Hold Signal:

The latency of the sample and hold from the LAT is 2 μ s, therefore, the minimum peaking time of the shaped pulse is 2 μ s. However, since the resistor and caps fabricated in silicon can vary by 20% from one run to another, the peaking time should be increased to $2 \mu\text{s}/0.8/0.8 = 3.125 \mu\text{s}$. A peaking time of 3 μ s has been chosen as the hold signal coming a little before the peak will not affect the linearity, but only reduce the gain slightly.

Therefore to sample the shaped signal at its peak value, the L1T trigger from the LAT should be delayed by 1us before sending it to the analog ACD ASIC. However, if the resistances and capacitors fabricated reveal that the actual value fabricated is 20% less than the designed, then the peaking time will occur at 2 us instead of 3us. For such cases the delay in the L1T trigger before it is applied as Hold signal to the

analog ASIC should be zero. Conversely, if the resistance and capacitance values fabricated are 20% over, then the peaking will occur at 4.7 μ s. In this case, the L1T trigger should be delayed by 4.7 - 2 = 2.7 μ s before it is applied as a hold signal to the analog ASIC.

Thus there should be an adjustable delay in series with the Hold signal going into the analog ASIC, this delay should be adjustable from 0 to 2.7 μ s.

5.2.2.2.25 Test Charge Injection

An on-chip test charge injection circuit will be included in the analog ASIC. The charge injection capacitor (internal to the analog ASIC) will have a value of approximately 16 pF. This will provide the following voltage-to-charge-to-MIP equivalence (for a nominal HLD threshold signal):

$$25 \text{ MIP} \Rightarrow (25)(10 \text{ pe}^-)(1.6022 \times 10^{-19})(400,000) = Q = 16 \text{ pC}$$

The charge injection circuit will be used for both aliveness tests and characterization of the FREE circuit card. The charge injection mode will be controlled via two mode bits, commandable from the FREE circuit card. The modes are described as follows:

CI Mode Bit 1	CI Mode Bit 0	Function
0	0	disabled
0	1	disabled
1	0	LO range enabled
1	1	HLD range enabled

Test Charge Injection Control Table

5.2.2.3 The charge injection circuit will have adjustable amplitude based on a 6-bit DAC voltage. This DAC is internal to the analog ASIC. The nominal rate of charge injection will be 1000 Hz when the circuit is enabled. In addition, the ACD electronics shall be capable of generating synchronous charge injection signals in response to broadcast commands from the AEM. Analog-to-Digital Converter

The ACD will utilize a commercially available MAXIM MAX145 analog-to-digital converter that is suitably qualified and screened. This part will be identical to the ADCs used on CAL and TKR, and will be provided to GSFC by SLAC.

5.2.2.3.1 Spectral Performance of the Analog to Digital Converter

The analog-to-digital converter shall have a serial interface, operate from a single +3.3V supply, dissipate less than 10 mW at 1 kHz, and be in a surface-mount plastic package. It will be identical to that used on the CAL and TKR subsystems. This part will be supplied to GSFC by SLAC. The analog-to-digital converter will have a resolution of at least 11 bits. The signal-to-noise ratio of the analog system shall be a minimum of 66 dB. The analog-to-digital converter will be activated by the FREE circuit card logic whenever the LLD fires, the signal chain is not busy from a previous event, and L1T is received from the AEM. The analog-to-digital conversion time shall be less than 10 μ s. The low energy range will be digitized for pulses that are below the threshold range-switching discriminator. The high energy range will be digitized for pulses that are above the that threshold. There will be a test mode in which both ranges will be digitized, for cross-calibration.

5.2.2.4 Digital-to-Analog converter

5.2.3 High Voltage Bias Supplies

The high voltage bias supplies (HVBS) are assemblies that provide an adjustable bias to all 18 PMTs on a board. These are low power, low volume power supplies and are required to provide a normalized gain for the analog signal. There will be one HVBS per FREE circuit card and each card has 18 analog channels.

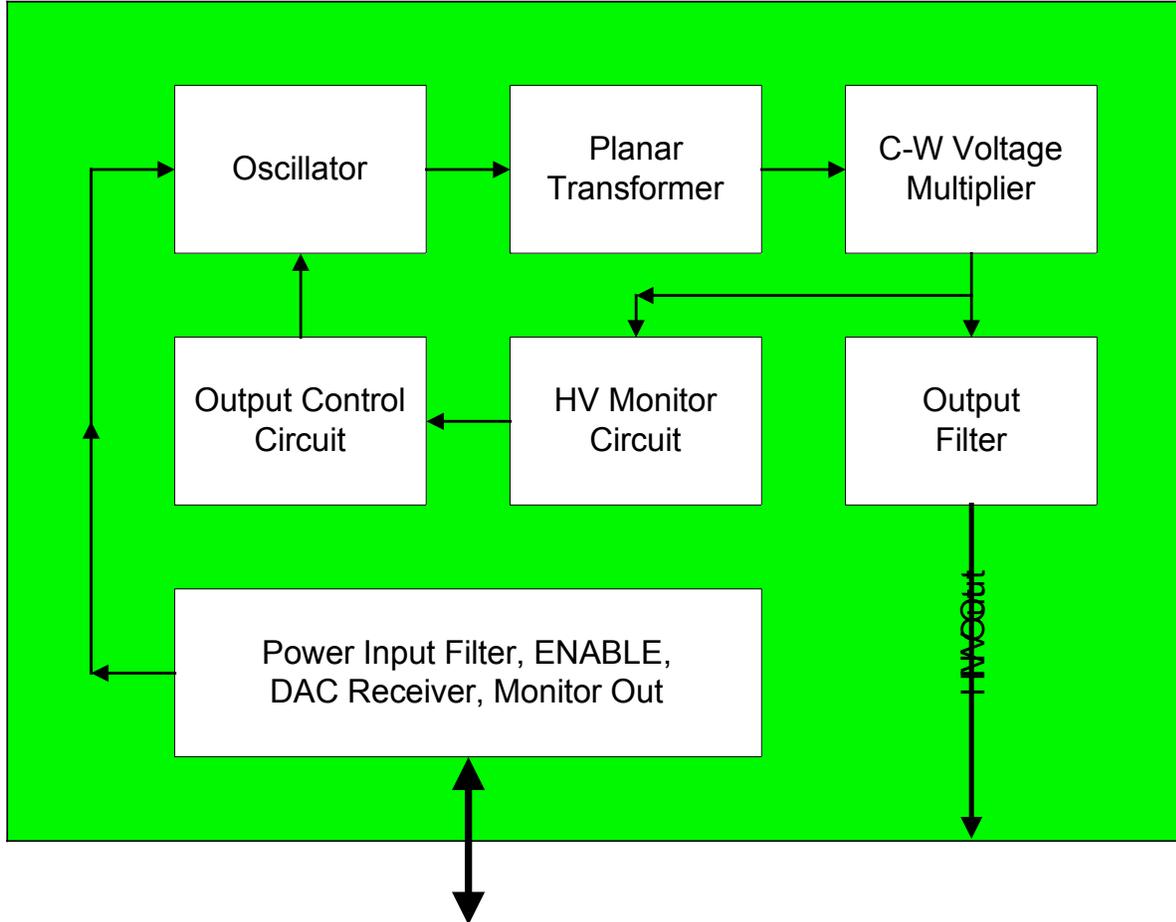
5.2.3.1 High Voltage Bias Supply (HVBS) Specification

HVBS Parameter	Minimum	Nominal	Maximum	LAT-SS-00352
Number of flight units		24		5.1
Number of PMTs load per flight unit		18		5.1
HV output voltage to be supplied	0	1000	1500	5.10.1
HV output current to be supplied (□A)		36	60	5.10.2
HV output current limit (□A)			80	5.10.3
HV output voltage adjustment	0V		2.5 V	5.10.4
Input power	22V	28V	34 V	5.10.5
Input Ripple			10 mV	5.10.5
HV Regulation Range Required	400V		1500 V	5.10.1
HV Line Regulation			0.5%	5.10.6
HV Load Regulation			0.5%	5.10.6
Ripple on HV output (RMS), 50 Hz – 50 MHz			2 mV	5.10.7
HVBS Power consumption			300 mW	5.10.8
Ramp up time constant	5 sec		30 sec	5.10.9
Ramp down time constant	5 sec		30 sec	5.10.9
Temperature stability			500 ppm/C	5.10.10
Temporal stability			0.05% / day	5.10.11
Output monitor	0		2.5 V	5.10.12
DC Isolation, HV Return to 28V Return	80 □	100 □	120 □	5.10.13
Oscillator frequency	100 kHz			5.10.14
Mass			150 grams	
Volume			TBD (Art)	
Output monitor output impedance		100 ohms (TBD Baker)		

5.2.3.2 Circuit Description

A block diagram of the HV topology is shown below:

High Voltage Bias Supply Concept



5.2.3.3 HVBS Assembly

5.2.3.3.1 PCB Layout

5.2.3.3.1.1 High Voltage Section

5.2.3.3.1.2 Planar Transformer

5.2.3.3.1.3 Low Voltage Section

5.2.3.3.1.4 Internal Shielding

The HV return shall be isolated from both chassis and HV supply ground (e.g., 28V RTN) by 100 +/- 20 ohms. The HV return shall be grounded to the analog ground at the PMT with a DC resistance of < 100 milliohms. The 100Ω resistor is utilized to break the ground loop that could be formed between the 28V HVBS power and the Event Processor 3.3V. The connection of the HV output ground to the FREE circuit card ground ensures that the high voltage output is AC-referenced to the photocathode/analog ASIC ground and not the primary side of the transformer in the HVBS.

The HVBS will be enclosed in a conductive housing to provide EMI/EMC shielding. The enclosure surfaces will be plated with a non-oxidizing conductor. A 1.5 ± 0.5 mm diameter vent hole will be provided in the housing to ensure rapid venting.

5.2.3.3.1.5 Coating and Staking

All flight electronics surfaces shall be conformal coated with a NASA-approved polymer. Uralane 5750 is one example of an approved coating material. Uralane 5753 is an approved staking compound.

5.2.3.3.1.6 Interfaces

5.2.3.3.1.6.1 Low Voltage Free Card Interface

5.2.4.2.1.6.2 High Voltage Output

5.2.3.3.2 Housing

5.2.3.3.2.1 Materials and Configuration

5.2.3.3.2.2 Mounting Method

5.2.3.4 Redundancy

5.2.3.5 Electrical Performance

5.2.3.6 Testing

5.2.3.6.1 Bench Electrical

5.2.3.6.2 Temperature

5.2.3.6.3 Corona

5.2.3.6.4 Vacuum

5.2.3.6.5 Environmental

5.2.3.6.5.1 EMC

5.2.3.6.5.2 Vibration

5.2.3.6.5.3 Thermal Vacuum

5.2.4.5.5 Life Testing

5.2.4 PMT Assembly

5.2.4.1 Photomultiplier Tubes

The photomultiplier tubes being used for the ACD will be Hamamatsu model R4443 tubes. These tubes are head-on, 1250 V (maximum) bias tubes with gain adjusted to ~400,000.

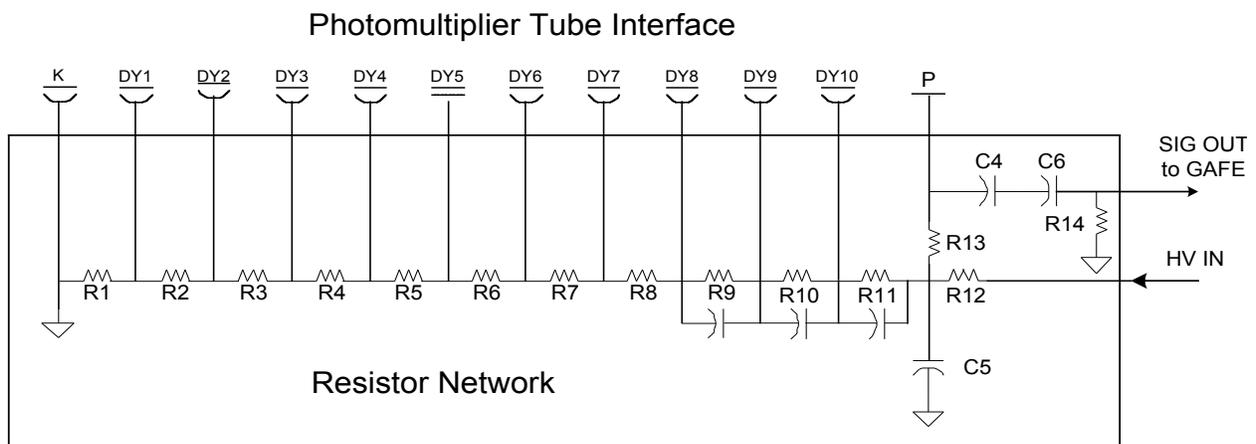
5.2.4.2 Photomultiplier Tube Biasing Circuitry

Each PMT requires a series of resistors and capacitors to be properly biased. The nominal bias string current is 2 μ A at 1250 V. The nominal current at the anode of the PMT (gain = 400,000) is calculated for a 1 kHz rate as

$$I = \frac{Q}{t} = \frac{(10pe)(1.6022 \times 10^{19})(4 \times 10^5)}{0.001s} = 640pA$$

The bias string current is purposely set high to allow for (1) a possible larger number of photoelectrons (x5) and (2) uneven gain degradation within a group of 9 PMT's, which would require higher gain for the stronger PMT's.

For a PMT with 10 dynodes, anode (K), and grounded photocathode (P), the following biasing circuitry is typical:



In this configuration, resistor values of approximately 75 M Ω are appropriate for the dynodes. The high voltage rated (2500V) capacitors are approximately 1000 pF. The current limiting resistor for the HV supply is also approximately 75 M Ω , providing a 150 V voltage drop at the nominal 2 μ A. [LAT-SS-000352, section 5.11.1 - 5.11.3]

The capacitor from resistor R13 to ground is a high voltage bias filter and meets the requirement of LAT-SS-00352, section 5.11.4.

In the diagram above, the resistor designated as R15 has a value of approximately 10 M Ω , as per LAT-SS-00352, section 5.11.5.

Additionally, resistor R14 has a value of 10 k Ω , as per LAT-SS-00352, section 5.11.6.

The capacitors bypassing R10, R11, and R12 meet the requirement of LAT-SS-00352, section 5.11.7.

5.2.5 FREE/HVBS/PMT Assembly Interface

5.2.5.1 FREE to HVBS Interface

5.2.5.2 FREE to PMT Interface

5.2.5.3 HVBS to PMT Interface

5.2.6 Timing

6 ACD FREE circuit card Environmental and Testing Requirements

6.1 EMI/EMC Specification

Electromagnetic interference characteristics per MIL-STD-461/462:

6.1.1 Conducted Emissions (CE03)

6.1.2 Radiated Emissions (RE02)

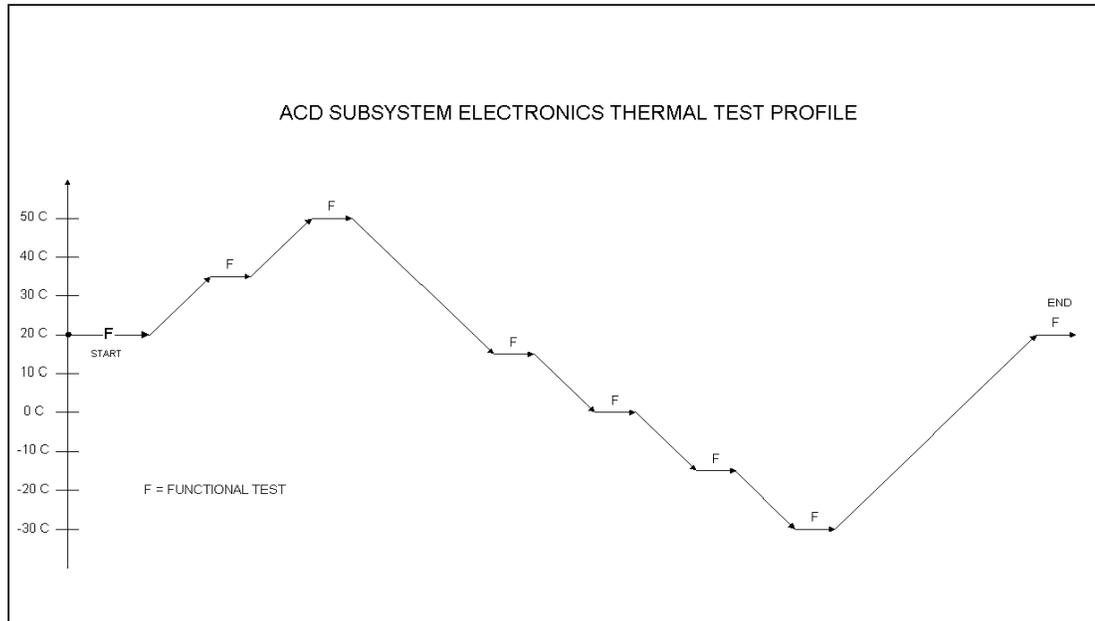
6.1.3 Conducted Susceptibility (CS02, CS03)

6.1.4 Radiated Susceptibility (RS03)

6.1.5 Magnetic Properties

6.2 Thermal Testing, Vacuum Testing, and Thermal Constraints

The nominal operating temperature range for the ACD electronics is from -10C to +40C. The survival (non-powered) temperature range for the ACD electronics is from -20C to +50C. Note that the PMTs must be kept below +50C at all times. The maximum thermal transition for the ACD electronics is 10 degrees C per hour. The electronics will be tested for functionality at the following temperatures in an ambient environment: 22C, 35C, 50C, 15C, 0C, -15C, -30C, 22C. The profile for subsystem thermal testing is as follows:



The HVBS will be thermal vacuum tested as assemblies prior to integration with other ACD flight electronics. The HVBS are not required to operate at atmospheric pressures between 0.1 and 800 millibars. The ACD FREE circuit card will be thermal vacuum tested with the ACD as a subsystem, not individually.

6.3 Structural and Mechanical Testing

The structural and mechanical testing is defined in the "LAT ACD Verification Plan" whose document number LAT-TD-00434

6.4 Electromagnetic Compatibility Testing

It is a requirement for the ACD electronics to neither generate nor be susceptible to electromagnetic interference exceeding the GLAST LAT EMI/EMC instrument specification. [LAT-SS-000xx-D1, section 5.10.15] The electromagnetic testing is defined in the "LAT ACD Verification Plan" whose document number LAT-TD-00434

6.5 Radiation Design Requirements for the Electronic Components

6.5.1 Total Ionizing Dose Tolerance

The ACD electronics will be radiation tolerant to a total dose of 2 krad/Si. With a safety factor of 5 applied, the components will be designed to withstand 10 krad/Si total dose for the mission duration. [LAT-SS-00352, section 5.12]

6.5.2 Latchup Tolerance

The ACD electronics will either not be susceptible to latchup, or, if susceptible, will autonomously detect a latchup and cycle power on the affected part. [LAT-SS-00352, section 5.13.3] The GLAST IRD requirement is SEU linear energy transfer sensitivity of better than 8 MeV cm²/mg.

6.5.3 SEU Tolerance

The ACD electronics will be tolerant of single event upsets such that, in response to a SEU, the electronics will not transition to an unsafe state. [LAT-SS-00352, section 5.13.4]

6.6 Operation Prior to Delivery

The ACD subsystem flight electronics shall be operated successfully for a minimum of 100 hours prior to delivery.

6.7 Electronics Cleanliness

The ACD subsystem flight electronics shall be kept in an ESD-safe (per NASA 8739.7) environment, handled with care, and kept clean. There is no specific cleanliness specification for the electronics beyond the LAT specification.